The experience of giving birth to a chip

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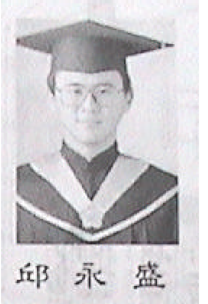
2003-12-10 / 邱永盛 于國立中山大學

The experience of giving birth to a chip

- Personal experience
  - 1992 畢業於成大電研所 CAD組碩士班
  - 1992~1994服役期間任雷達教官一職
  - 1994 加入揚智科技 Chip-Set部門
  - M1535 Project-Leader
  - 2002 轉戰通訊部門
  - M4301A Project-Leader
  - Now, a new project’s Product Manager

11年前



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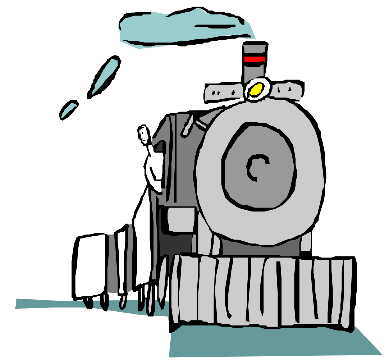
The experience of giving birth to a chip

- 二個中山電研所學生與二個中山資工所學生一起搭火車參加一場論文研討會。



- 去程，二個中山電研所學生買了二張票，二個中山資工所學生卻只買了一張票。

??? ??

一張票

二張票

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The experience of giving birth to a chip

- 查票時，二個中山資工所學生躲進一間廁所・・・

- 回程時，二個中山電研所學生了解了並買了一張票，但二個中山資工所學生卻不買票。

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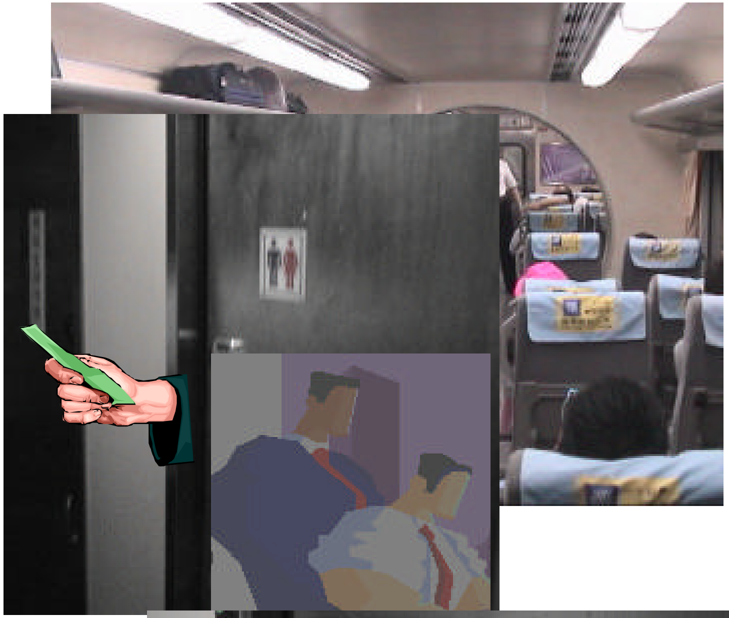
The experience of giving birth to a chip

- 查票時，二個中山電研所學生躲進一間廁所．．．



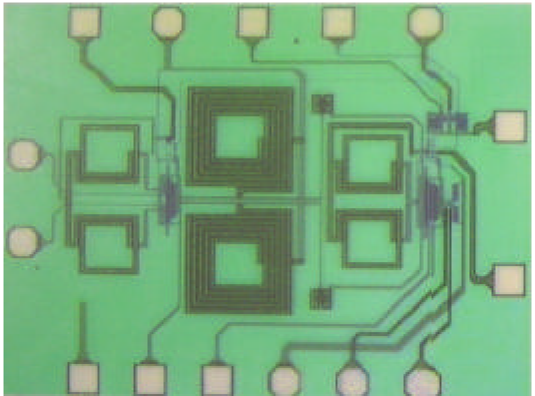
- 中山資工所學生跑去敲門，拿走車票後躲進了另一間廁所。

The experience of giving birth to a chip

- 唯一不會變的一件事：就是"變"
  - Process
  - EDA Tools
  - Design
  - Chip's Complication

閉關練功

- Gentleman : Let's start to incubate a chip.
  - Focus on digital design.



The experience of giving birth to a chip

- ***Environments Evaluating***
- ***Specification & Architecture Defining***
- ***Chip-Level Planning & Implementing***
- ***Verifying & Maintaining***
- ***Conclusion***

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1. Environments Evaluating

- Outside Environments

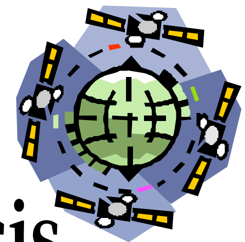
  - Marketing, Fab., Package consideration

- Inside Environments

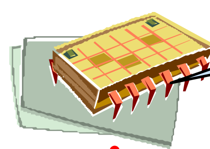
  - In-house Capability

1. Environments Evaluating

- Outside Env.
  - Marketing :
    - ~ Competitor's analysis
    - ~ Customer's requirements



情報蒐集



- 專利問題迴避

專利≠發明

專利≅給對手的絆腳石

1. Environments Evaluating(cont.)

- Fab & Fab's process decision :

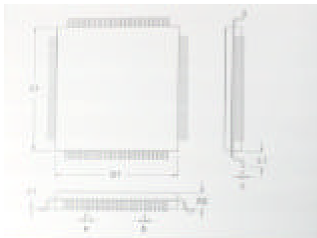
~An example for UMC 0.18u & 0.22u process decision.

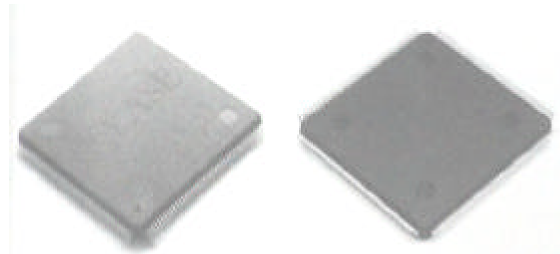
process	0.18u camps say	0.22u camps say	Notes
Die Area & Cost	1. Maybe cost little more than 0.22u process.	1. 0.18u do not save cost. 2. If this design is not wide enough, it will cost much for further several times digital ECO.	* In [illegible]'s architecture, analog parts and RAMs are occupied most of the die's area. So, 0.18u process do not gain the advantages of cost.
PADs	1. There are 30% Low-Fatter PADs supporting to save die's area.	1. The Low-Fatter 0.18u PADs still have ESD problem, now.	* In 0.22u process, we may only one choice : the standard UMC 0.25u PADs [Note1]
Process mainstream	1. 0.18u will be the mainstream at year 2004. 2. [illegible] had recommended us to use 0.18 at all. 3. Be afraid of the capacity problem for 0.25u process.	1. Capacity shouldn't be so critical even at the end of 2004. There is no reason to think UMC will drop 0.25 process two years later.	
Process stability	1. 0.18u process's stability problem should be solved in the future.	1. Why do we need to take the uncompromised risk.	* Now, based on my getting informations, the process stability issue is still not solved, e.g. Agilent [illegible]
USB 2.0 PAD (PHY included)	1. 0.18u test chip & [illegible] can do previous verify before [illegible] integration.	1. We can make sure the 0.22u process's USB IP already be well ready for using and for mass production.	
Power consumption	1. Nevertheless, 0.18u process can save power for core only need 1.8 volt.	1. 0.18u process save little power for most of the analog still use 3.3 volt as the power source, and it consume most of the power in the chip. If it saves little while comparing with RF's consuming, it will be meaningless.	
Timing Budget	1. [illegible] had been suffer the timing budget's trouble under 0.25u process. 0.22u process will be impossible for it is 10% timing worst than 0.25u process.	1. Under 0.22u process, adding should not be so critical for timing concern while co-working with Layout. Otherwise, it is design's issue and should solve on design phase, not via new process to pay more.	* SW team prefer to choose between 0.25u and 0.18u for the timing issue [Note2]
PLL	1. Need to modify for 0.18u process with risk.	1. Use the [illegible] PLL and assume it to be ready for use without risk.	

1. *Environments Evaluating(cont.)*

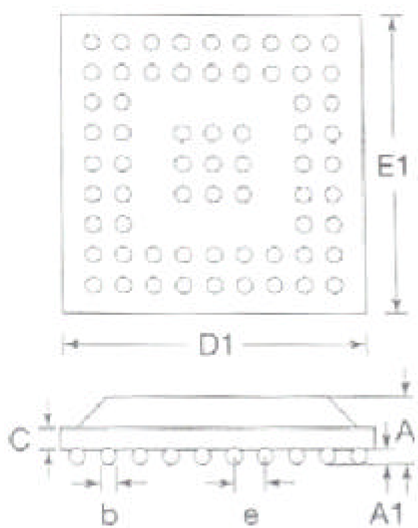
- Package technology suitable for using:

~ **QFP :**





~ **BGA :**



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1. Environments Evaluating(cont.)

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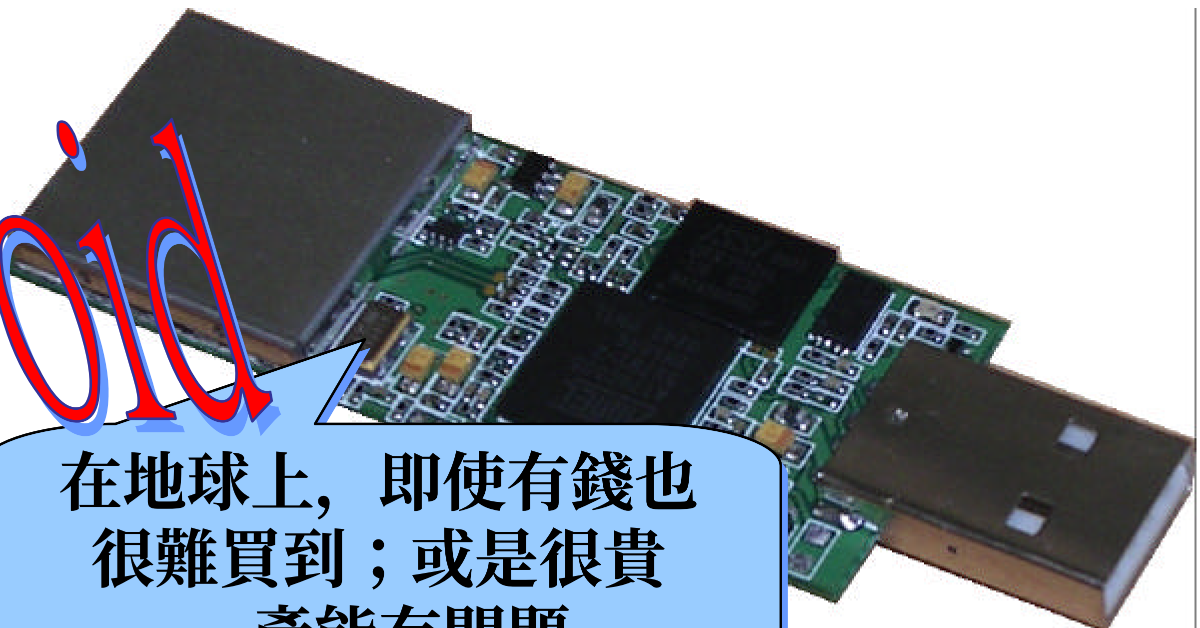
1. Environments Evaluating(cont.)

- Consider about the essential devices ：



Avoid

在地球上，即使有錢也
很難買到；或是很貴
、產能有問題

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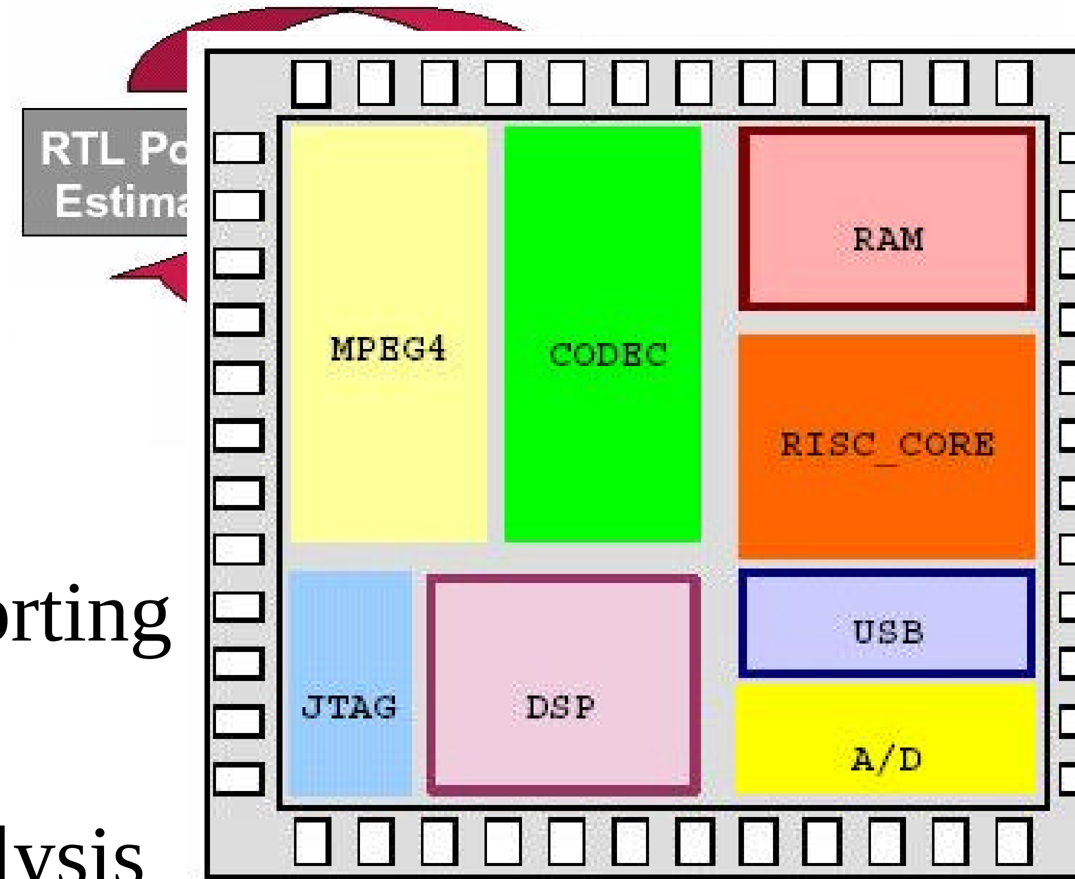
1. Environments Evaluating(cont.)

- Inside Env.
  - Design Flow
  - IP
  - Software Supporting
  - Testability Analysis



2. Spec. & Arch. Defining

- Firm the chip's specification

- Well defining the chip's architecture

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2. Spec. & Arch. Defining

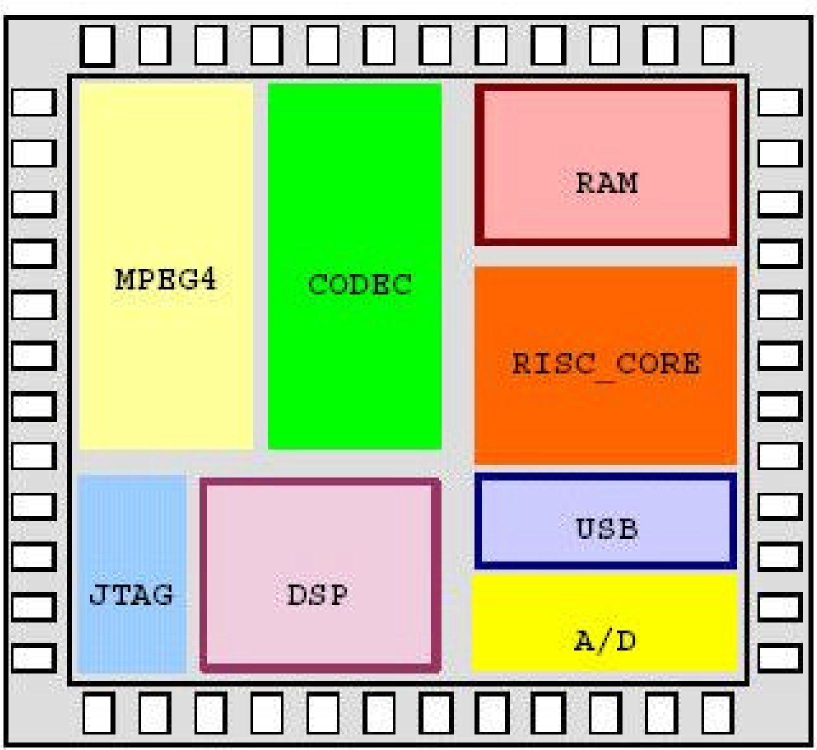
- Firm the chip's :
  - process
  - package
  - pin-out
  - feature

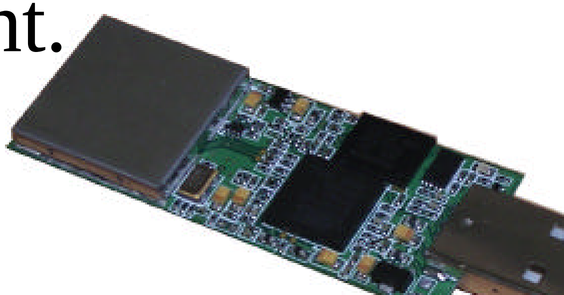
    For example :

    ~ Power by Battery ?

    ~ Working Temperature ?
  - power consumption requirement.

    ~ Under the system's point of view.

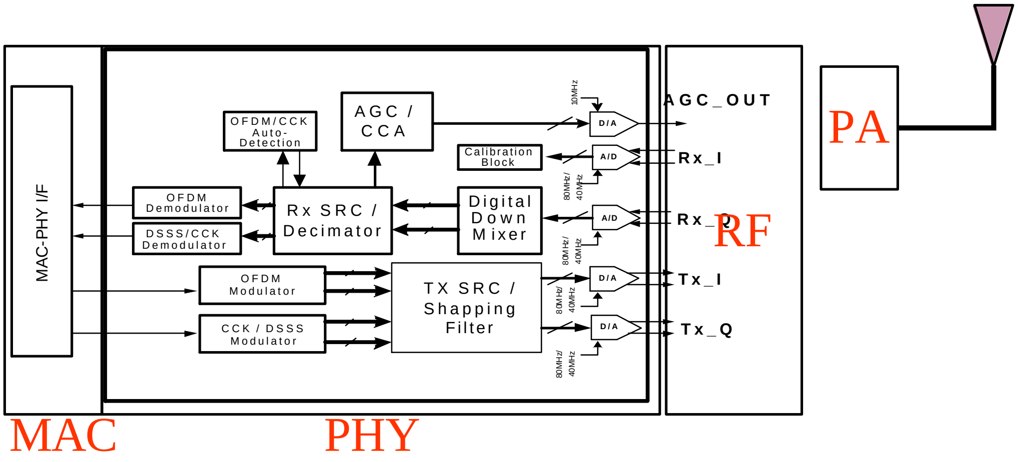




2. Spec. & Arch. Defining *(cont.)*

- Come out the chip's architecture

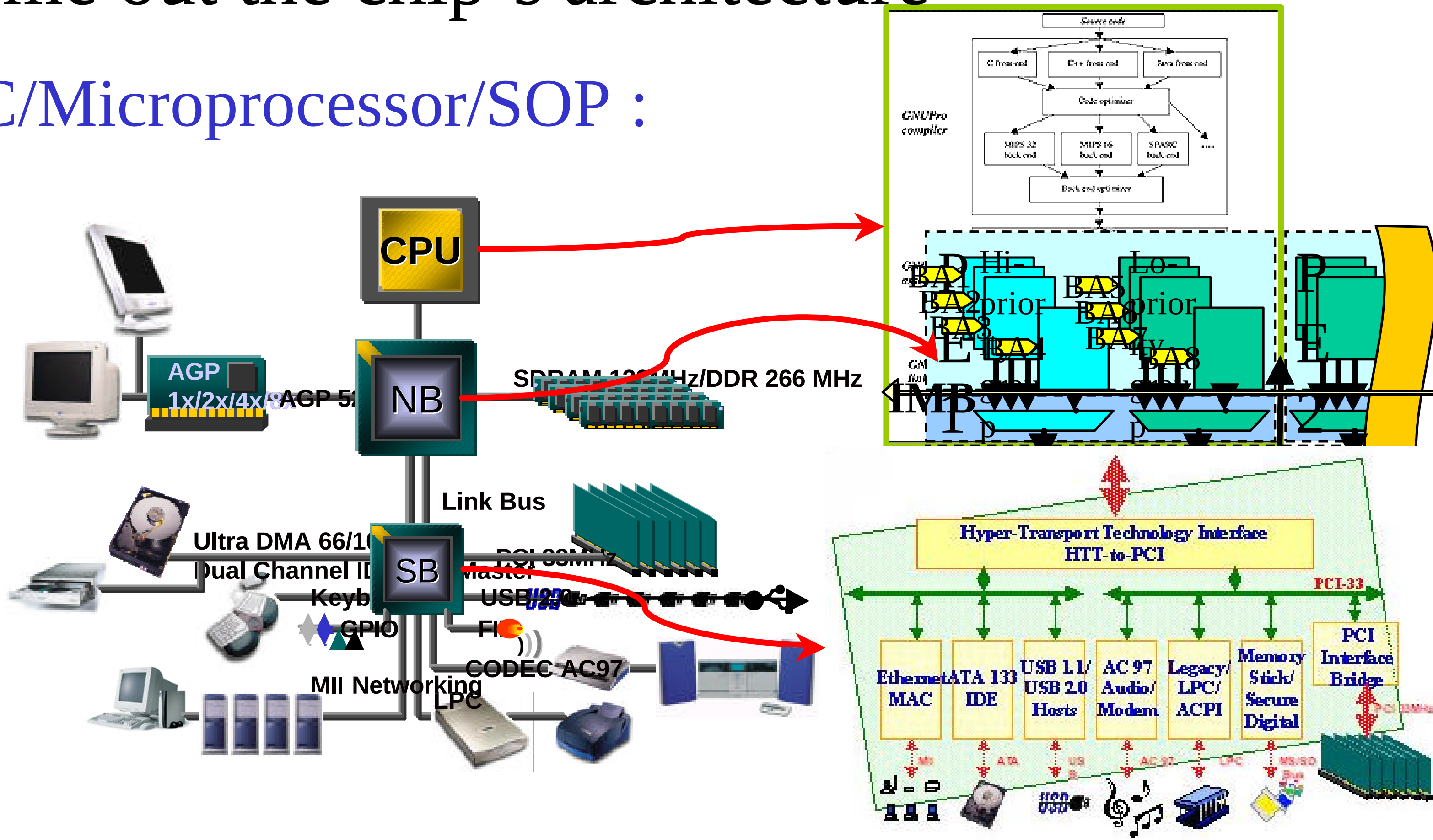
Network :



2. Spec. & Arch. Defining (cont.)

- Come out the chip's architecture

PC/Microprocessor/SOP :



3. Chip-Level Planning & Implementing

- The Designs
- Simulation & Synthesis
- Link to Layout
- Tape Out

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3. Chip-Level Planning & Implementing

- Design reuse, upgrade or new implement

  - Hard macros :

    1). Memory

      ~ Full Custom

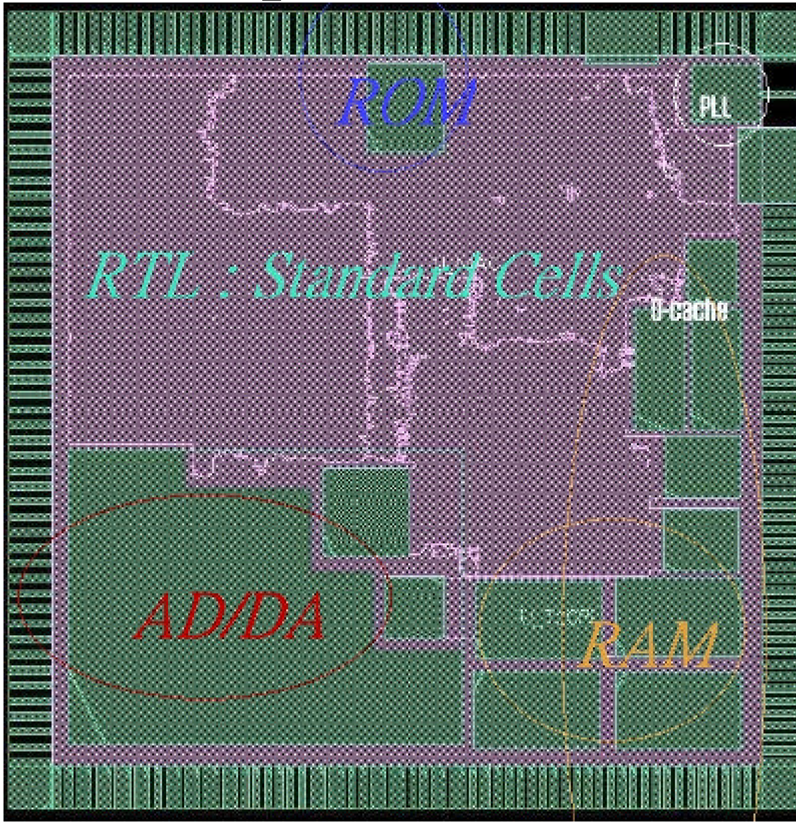
      ~ RAM/ROM Compiler

      ~ Mask ROM

      => without bist supporting

      ~ Flip-Flops/Latches

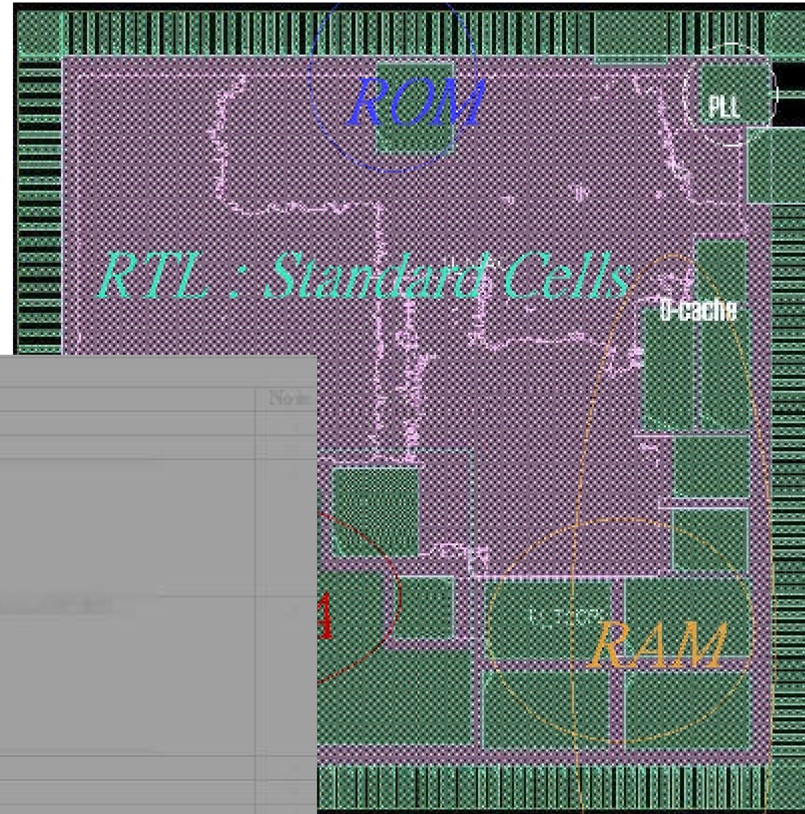
      ~ 1-T SRAM



3. Chip-Level Planning & Implementing(cont

2). Analog blocks : AD/DA, PLL etc…

- ~ Pin-out & Pin-location
- ~ Interface timing & loading
- ~ Frame view
- ~ specification review & check



TXDAC Parameters

	Min	TYP	Max	Unit	Description	Note
Analog Supply Voltage	3.0	3.3	3.6	V		
Temperature	0		125	C		
Output Common mode Voltage	1.15 0.5 1.3 0.5	1.25 1.0 0.25 1.4 1.2 0.8	1.35 1.5 1.4	V	[illegible]	
Full Scale Output Voltage Range		1.0 1.0 0.4 0.8 0.4 0.1 0.883		Vpp Vpp Vpp Vrms Vrms	[illegible]	
Sample Rate			44	MHz		
Max. Output Current	5	10		mA	Selected by IPS	
Output impedance		Hi-Z		Ohm		
Resolution		10		bit		
ENOB (Effective Number of Bits)		9		bit		
AC/DC Coupled		DC				
DNL (Differential Non-Linearity)	-1		+1	LSB		
INL (Integral Non-Linearity)	-1		+1	LSB		
Latency		1.5		T		
Time from PD to Normal Operation			0.5	mS		
Time from Sleep to Normal Operation			1	uS		

3. Chip-Level Planning & Implementing(cont

-RTL :

1). New coding

~ HDL : VHDL vs. Verilog

~ Coding Style

2). Modifying

~ Bug Solving

~ Spec. upgrade :

=> New version of spec. USB1.1 -> USB 2.0 PCI2.3 -> PCI-Express

=> Performance, Bandwidth enhancement. CD-RW 8X,20X …

=> Power save requirement. Power Saving ←→ Risk

3. Chip-Level Planning & Implementing(cont

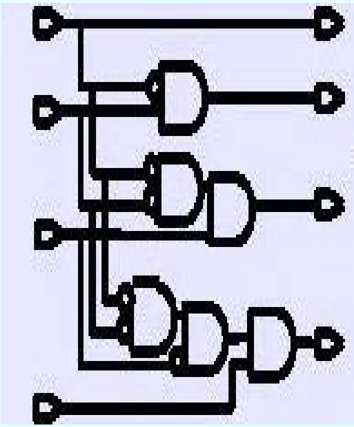
- Simulation & Synthesis
  - RTL & Gate-Level Simulation:
    - ~ Recently tools support co-simulation :
    - => Verilog-RTL, VHDL-RTL, Cells-Map and Gate-Level

```
Verilog
Reg [7:0]  queue;
Reg [2:0]  index;
...............
always @(.......)
begin
  ...............
  queue[index] <= 1'b1;
end
```

```
VHDL
signal queue : std_logic_vector
(7 downto 0);
signal   index   :   std_logic_vector
( 2 downto 0);
...............
process (.....)
begin
  ...............
  queue(conv_integer(index))   <=
'1';
end process;
```

```
component AND3X4
   Port (      A : In    STD_LOGIC;
               B : In    STD_LOGIC;
               C : In    STD_LOGIC;
               Y : Out   STD_LOGIC );
 end component;

 L_19 : AND3X4
     Port Map ( A=>CPU_FINISH,
B=>LDT_MODEL_CMD_FINISH,
C=>COMMAND_FINISHED,
Y=>ALL_FINISH );
```

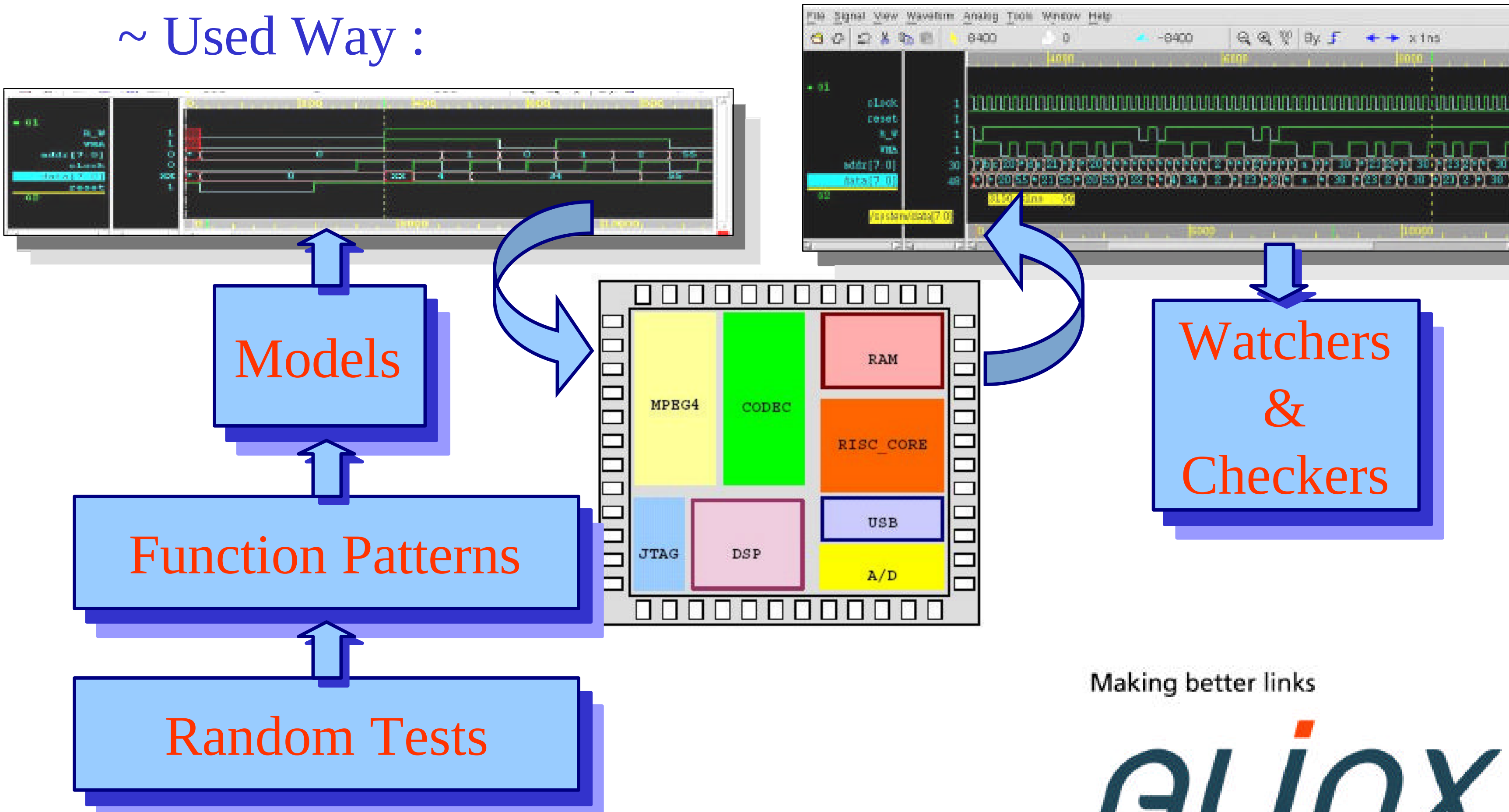


=> Modelsim, NC-Verilog …

3. *Chip-Level Planning & Implementing(cont*

- Simulation env., Timing check & (DFT) Design for Test:

~ Used Way :



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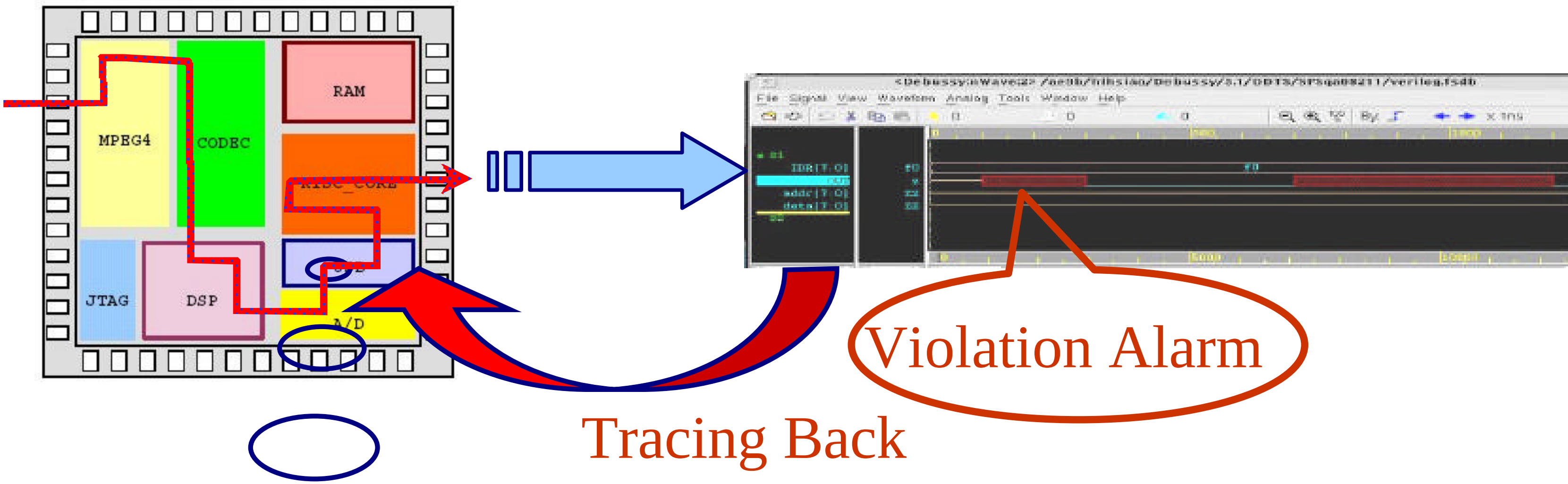
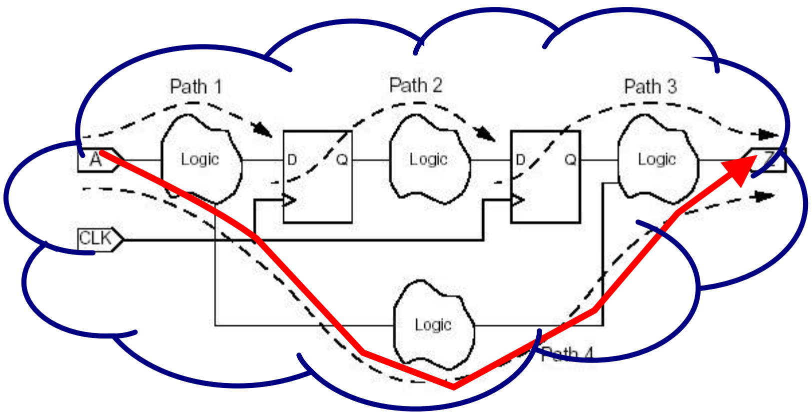
3. Chip-Level Planning & Implementing(cont

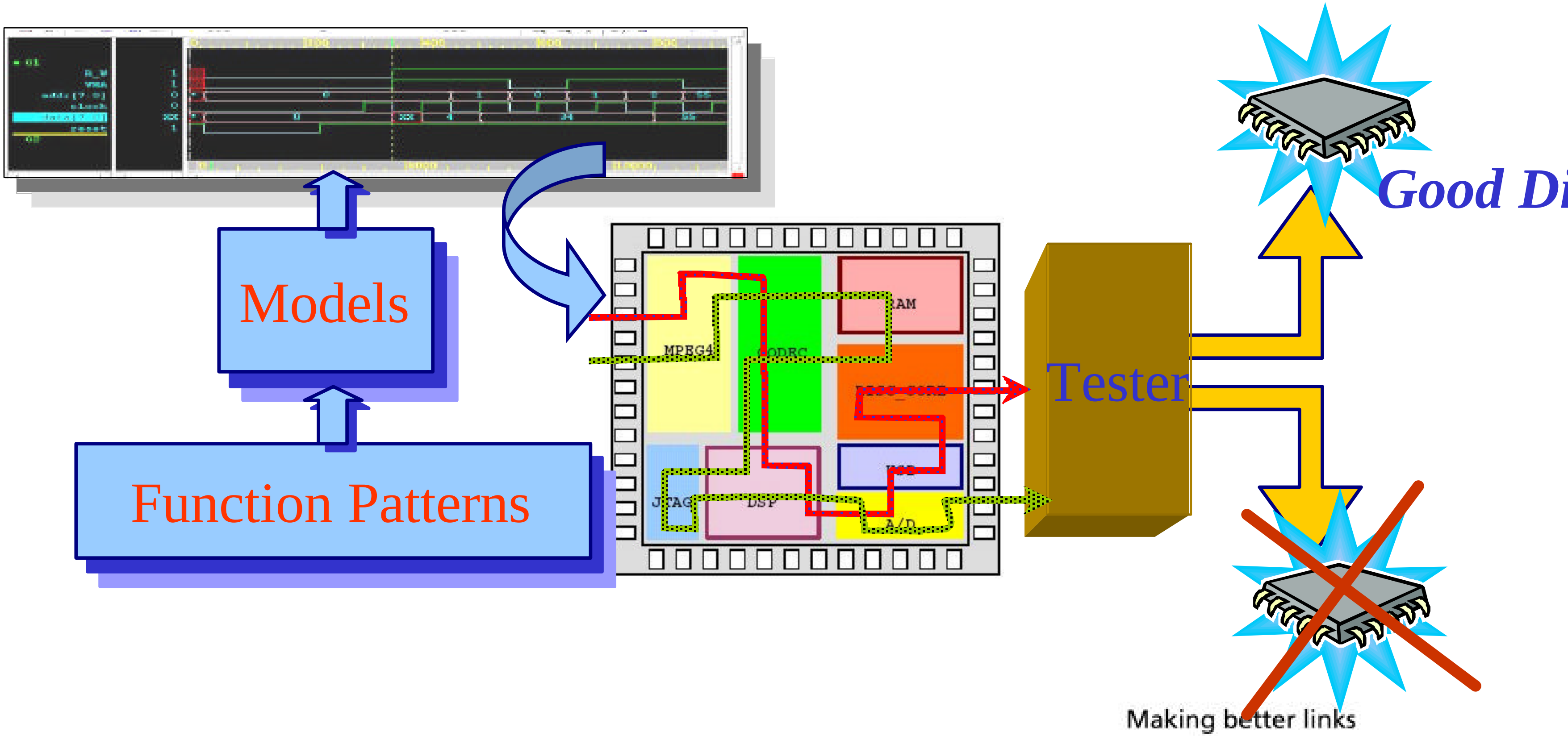
=> Only do partial paths' Timing-check by function patterns.





3. Chip-Level Planning & Implementing(cont

=> On the tester's final-testing relays on function patterns.



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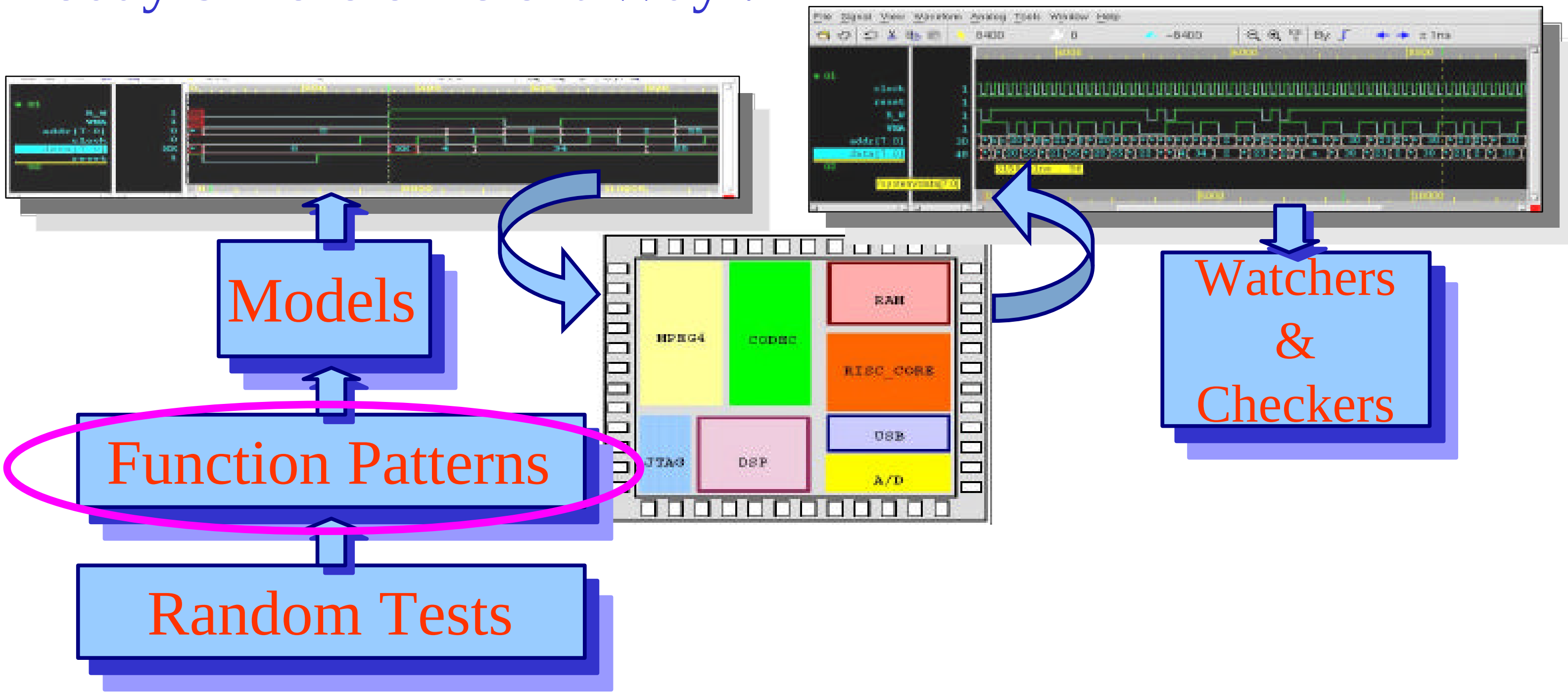
3. Chip-Level Planning & Implementing(cont

~ Today's more efficient Way :



⇒ Function Patterns still needed.

⇒ STA (Static Timing Analysis)

⇒ DFT (Design for Test)

by inserting scan-chain

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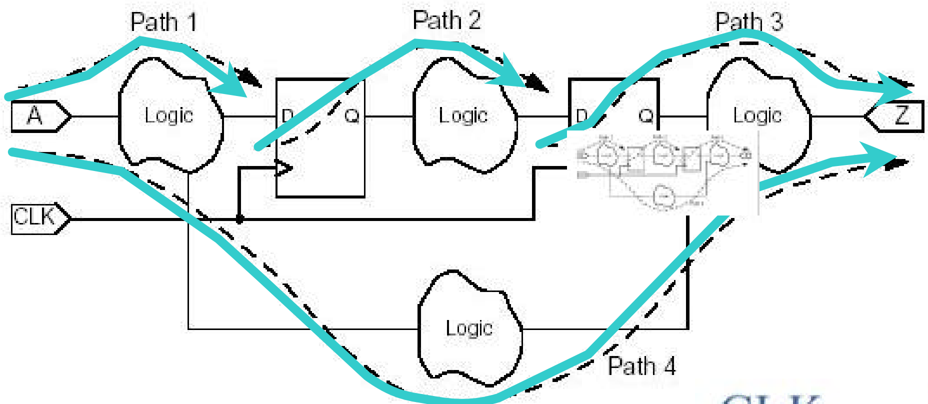
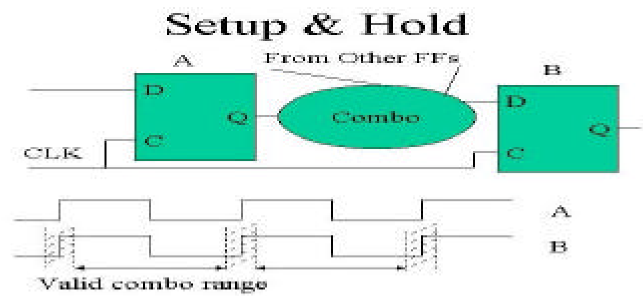
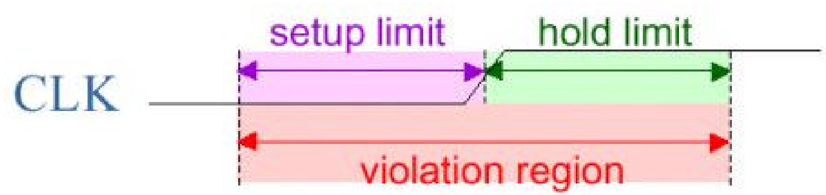
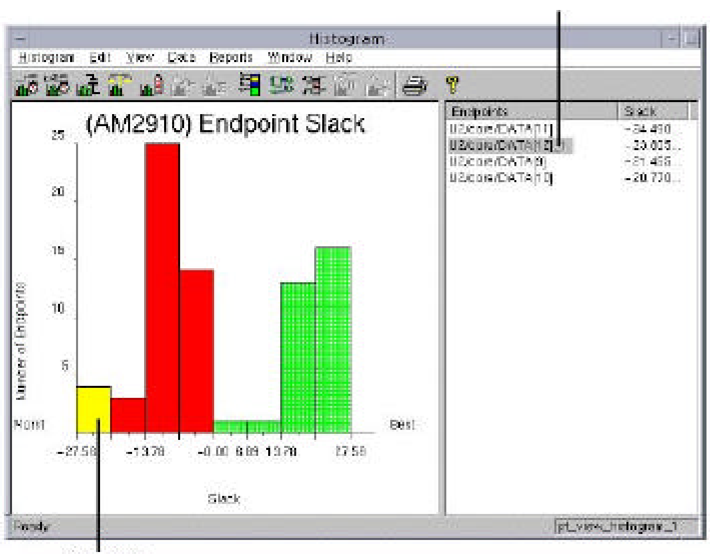
3. Chip-Level Planning & Implementing(cont

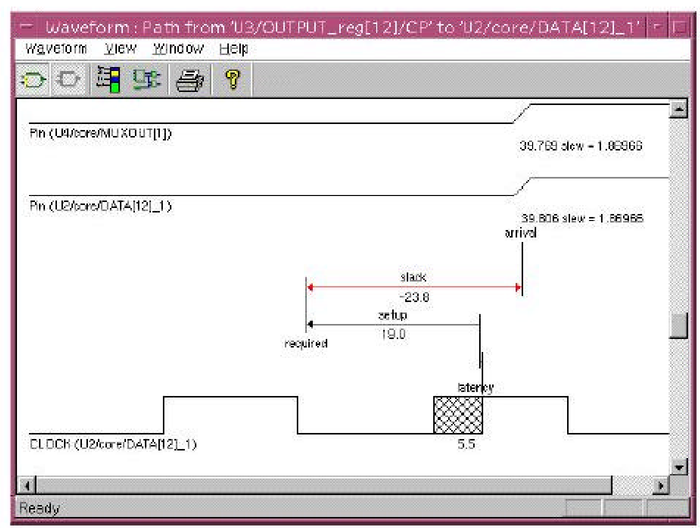
⇒ STA (Static Timing Analysis)







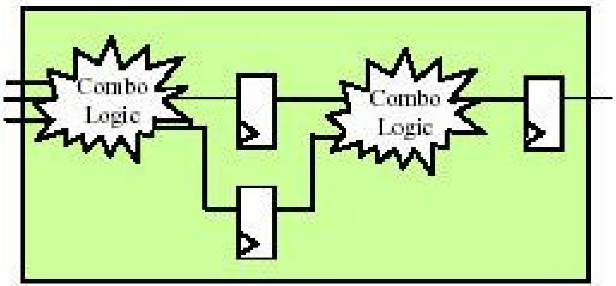




3. Chip-Level Planning & Implementing(cont

⇒ DFT

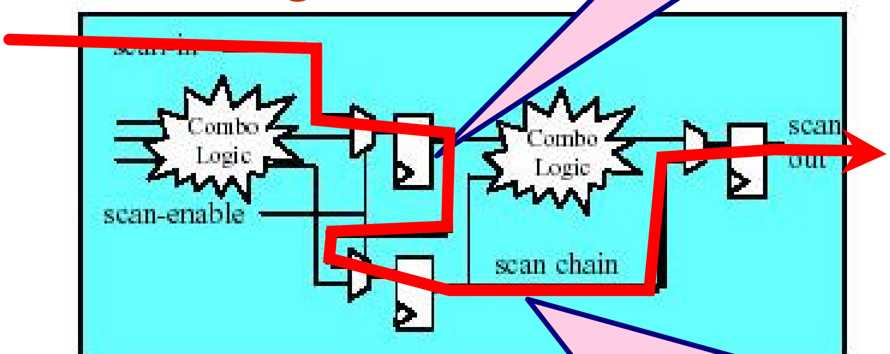
Design without Scan



Tester

1. Use Scan-Cells

Design with Scan



3. ATPG to gen. tester patterns

2. Insert Scan to build scan chain

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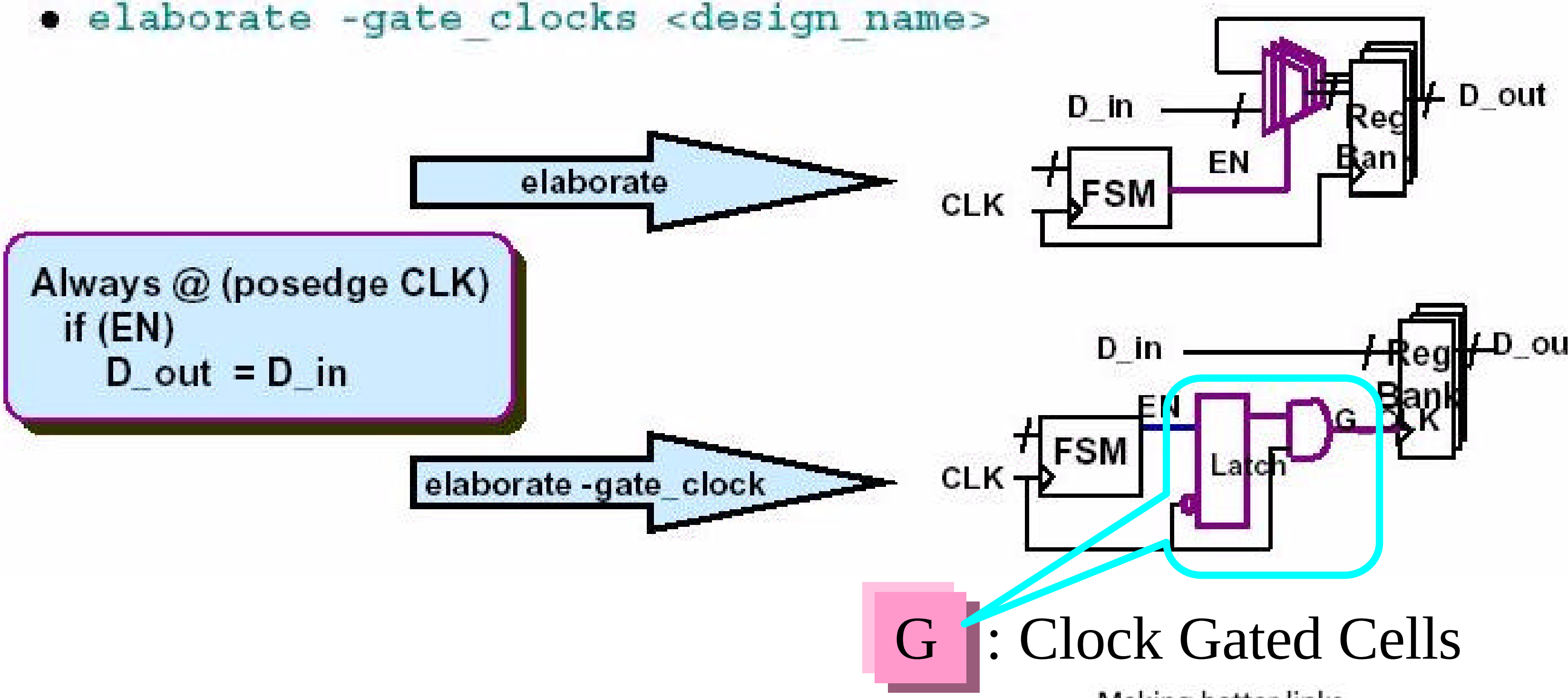
3. Chip-Level Planning & Implementing(cont

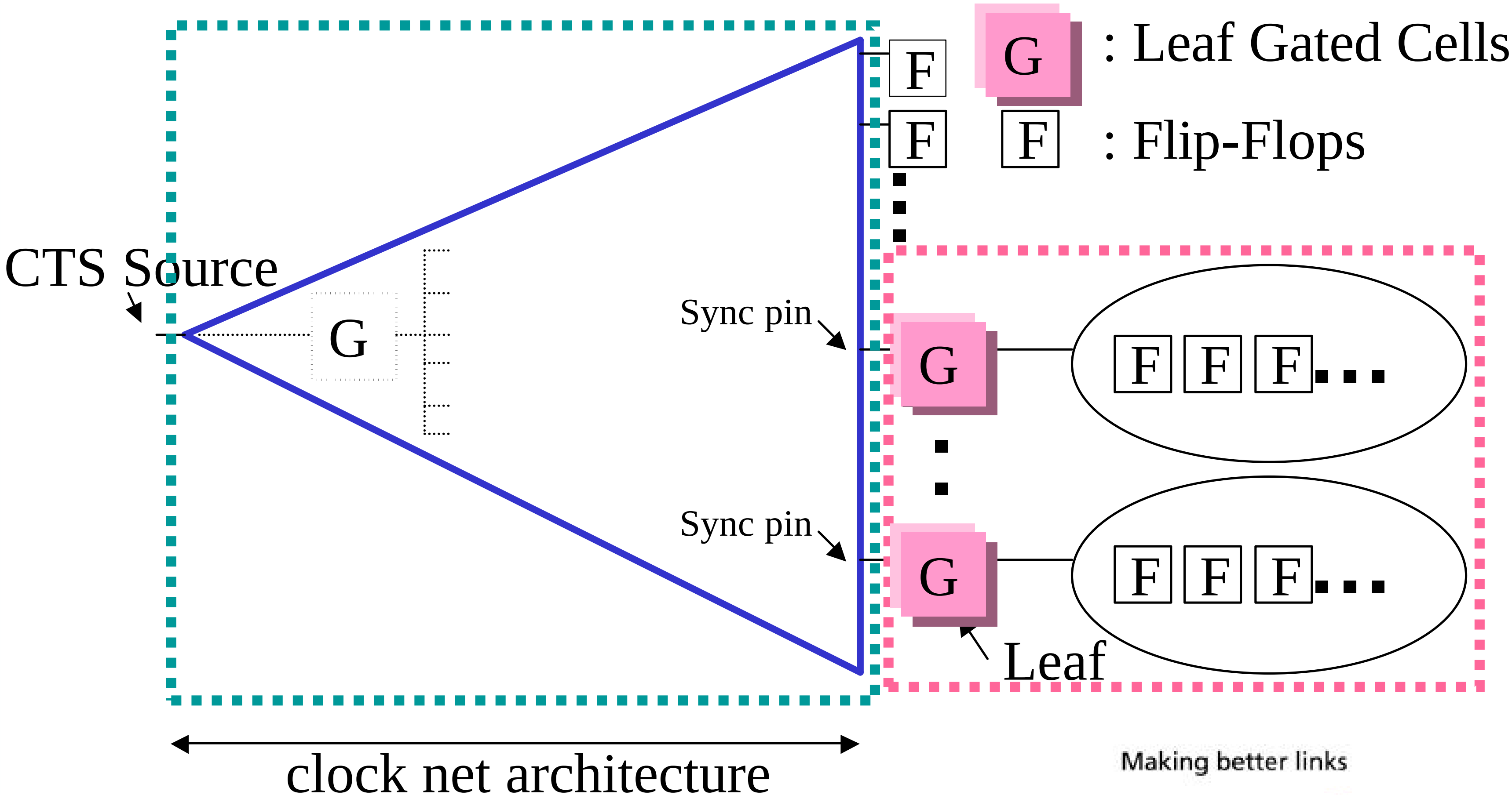
- Synthesis with Power Compiler:

- `set_clock_gating_style`
- `elaborate -gate_clocks <design_name>`



3. Chip-Level Planning & Implementing(cont

⇒ Architecture of CTS changes to be more complex.



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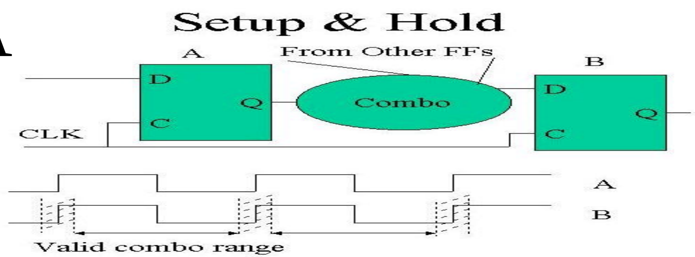
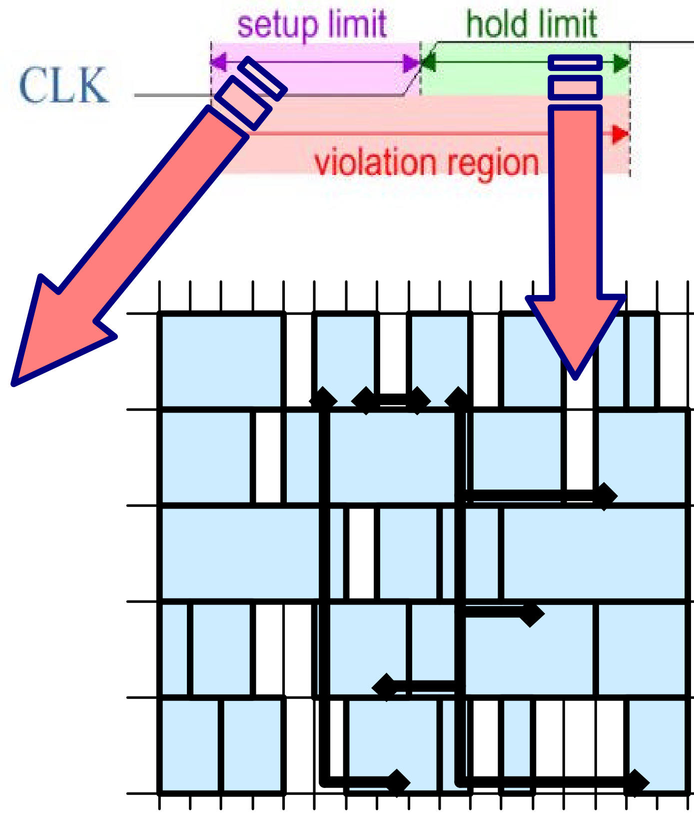
3. Chip-Level Planning & Implementing(cont

- Link to Layout
  - STA




```
Startpoint: I_DATA_PATH/Oprnd_A_reg[6]
            (rising edge-triggered flip-flop clocked by Clk)
Endpoint: I_ALU/Zro_Flag_reg
          (rising edge-triggered flip-flop clocked by div_clk)
Path Group: div_clk
Path Type: max
Point                                              Incr       Path
-----------------------------------------------------------------------------
clock Clk (rise edge)                              4.00       4.00
clock network delay (propagated)                   0.85 &     4.85
I_DATA_PATH/Oprnd_A_reg[6]/CLK (fdmf1c6)           0.00       4.85 r
I_DATA_PATH/Oprnd_A_reg[6]/QN (fdmf1c6)            0.64 &     5.49 f
I_DATA_PATH/Oprnd_A[6] (DATA_PATH_test_1)          0.00       5.49 f
I_ALU/Oprnd_A[6] (ALU_test_1)                      0.00       5.49 f
I_ALU/add_75_plus_172_dp_I65/CO1 (facs3a3)         0.16 &     5.65 r
I_ALU/add_75_plus_172_dp_U25/Y (clk1a3)            0.28 &     5.93 r
…
I_ALU/U411/Y (or4a3)                               0.29 &     8.18 f
I_ALU/U303/Y (and2c9)                              0.15 &     8.33 r
I_ALU/Zro_Flag_reg/D0 (fdesf1a2)                   0.00 &     8.33 r
data arrival time                                             8.33

clock div_clk (rise edge)                          8.00       8.00
clock network delay (propagated)                   1.53 &     9.53
I_ALU/Zro_Flag_reg/CLK (fdesf1a2)                             9.53 r
library setup time                                -0.33 &     9.20
data required time                                            9.20
-----------------------------------------------------------------------------
data required time                                            9.20
data arrival time                                            -8.33
-----------------------------------------------------------------------------
slack (MET)                                                   0.87
```



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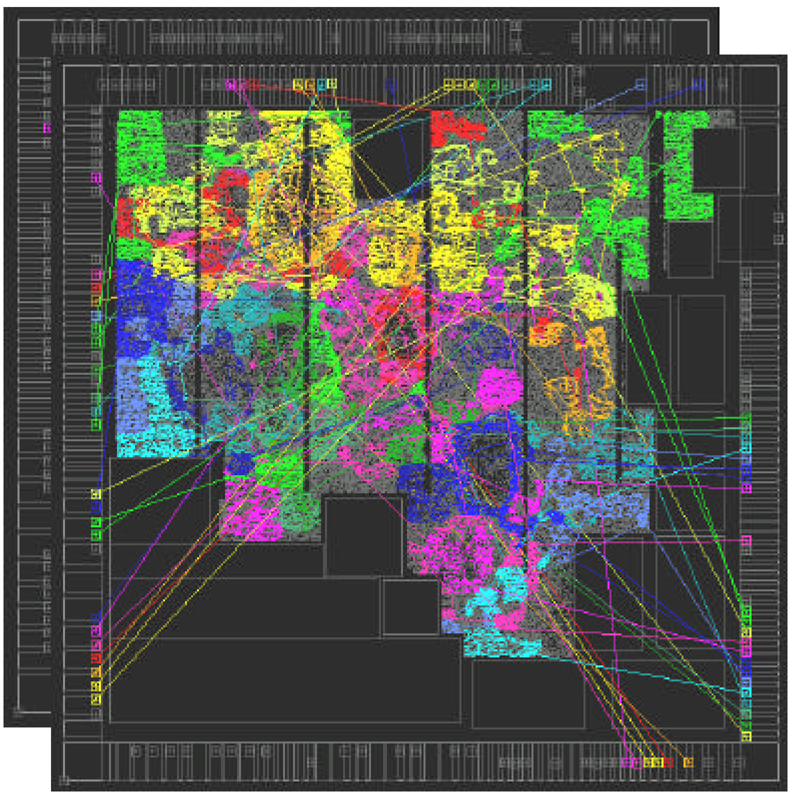
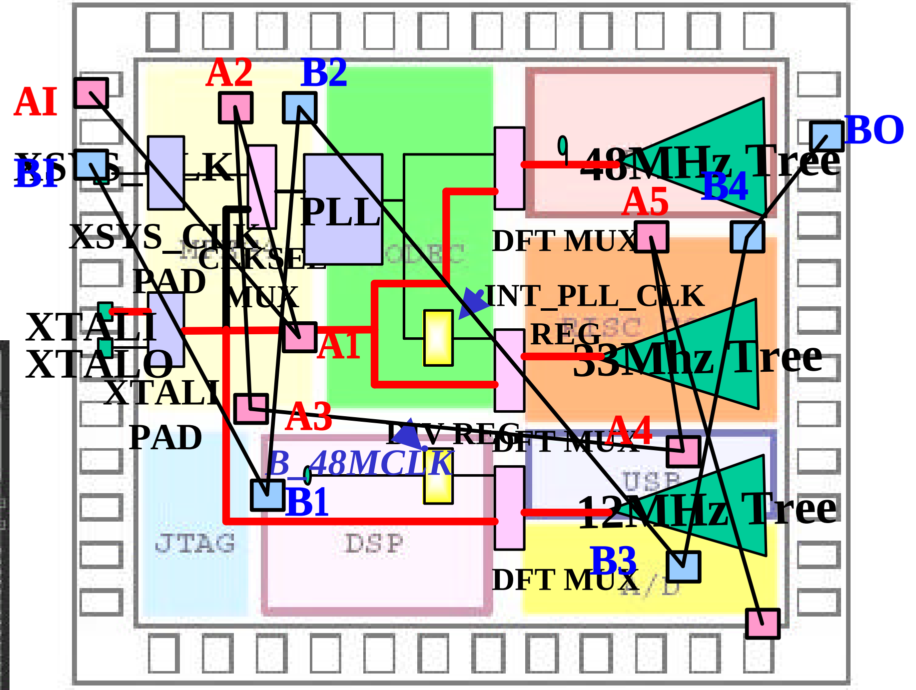
3. Chip-Level Planning & Implementing(cont

- CTS
- DFT : Scan Chain Partition





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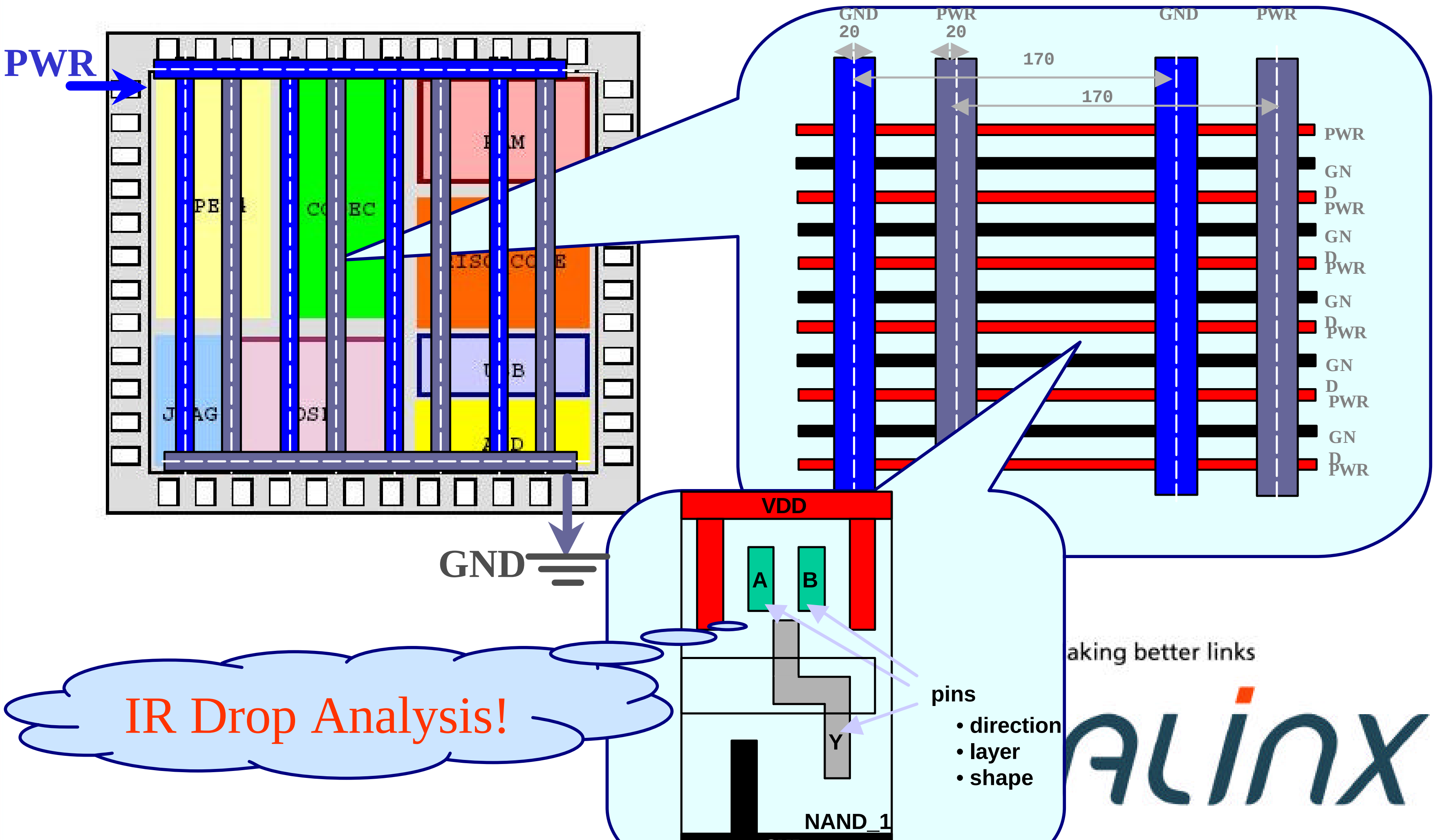
3. Chip-Level Planning & Implementing(cont

- Floor Planning, PAD Sequence, PAD and Core Power/Ground Assignment



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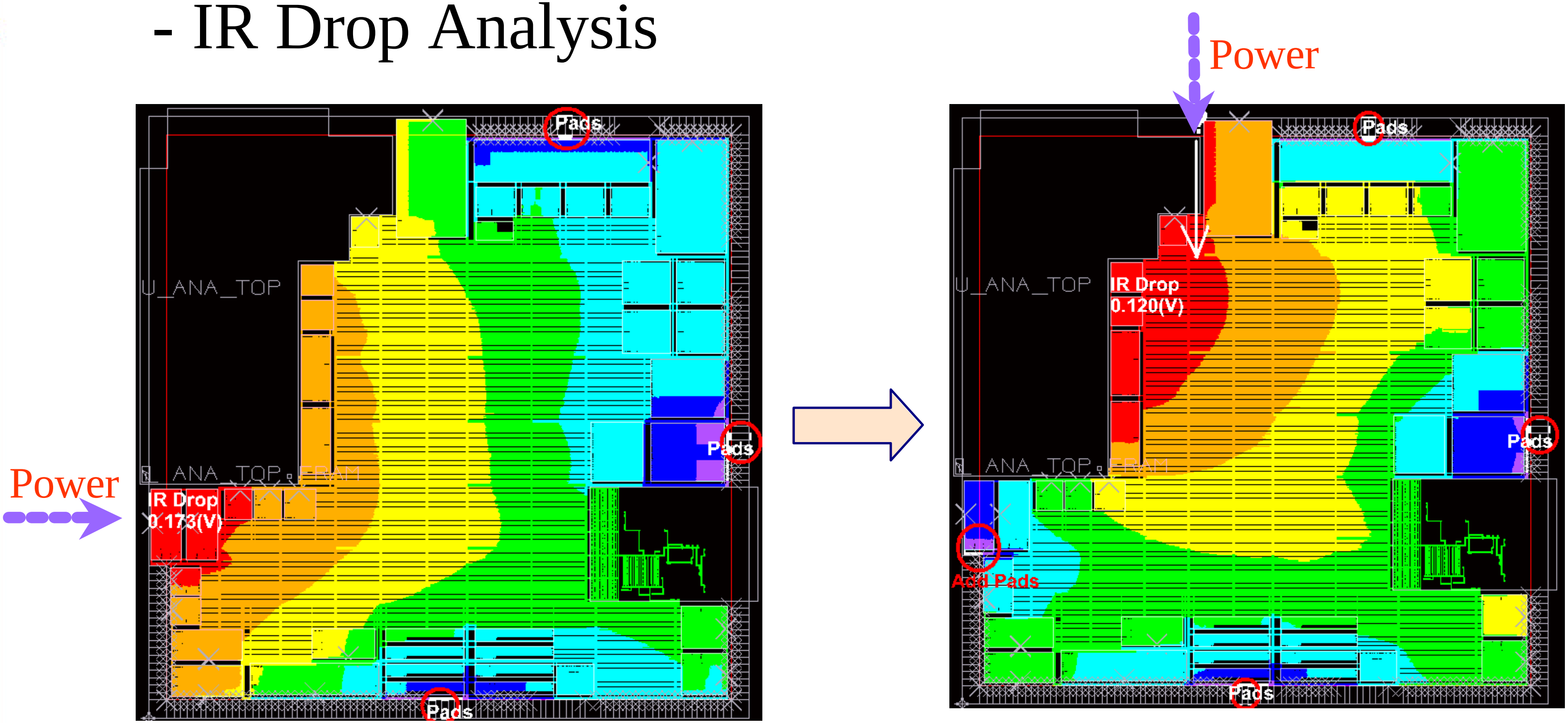
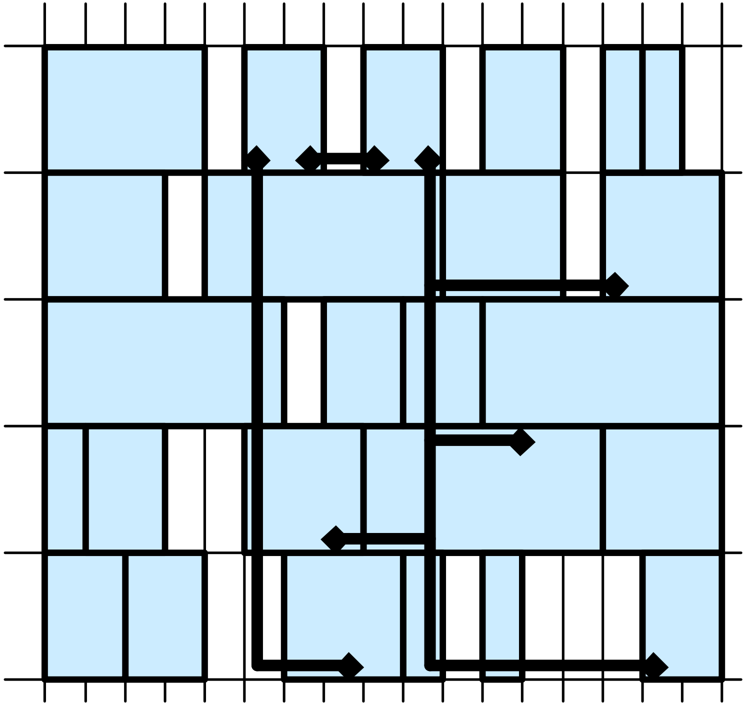
3. Chip-Level Planning & Implementing(cont

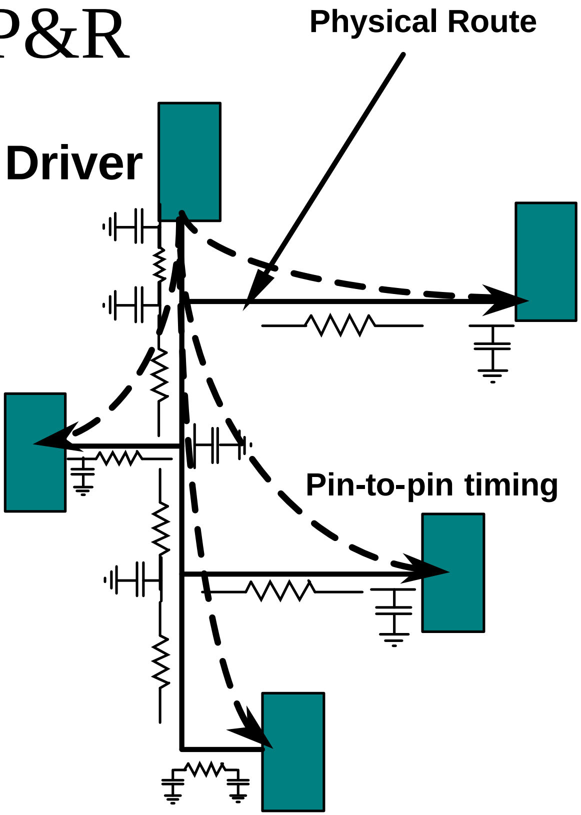
- IR Drop Analysis



3. Chip-Level Planning & Implementing(cont

- Link back to Front-End after P&R





~ STA (Static Timing Analysis)

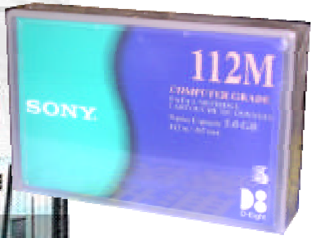
~ Post Simulation

~ Formal Check (Gate vs. Gate-Level)

Making better links

3. Chip-Level Planning & Implementing(cont

- Tape Out



MIS Backu

~ Database Backup

~ 拜拜

~ Send GDS file to Fab.

Making better links

4. Verifying & Maintaining

- Many Boards
- Yield-Rate Analysis
- Instruments / FIB / EMMI
- ECO
- Customer Supporting

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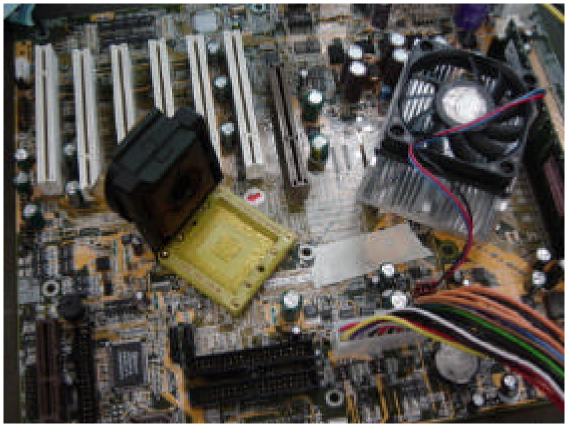
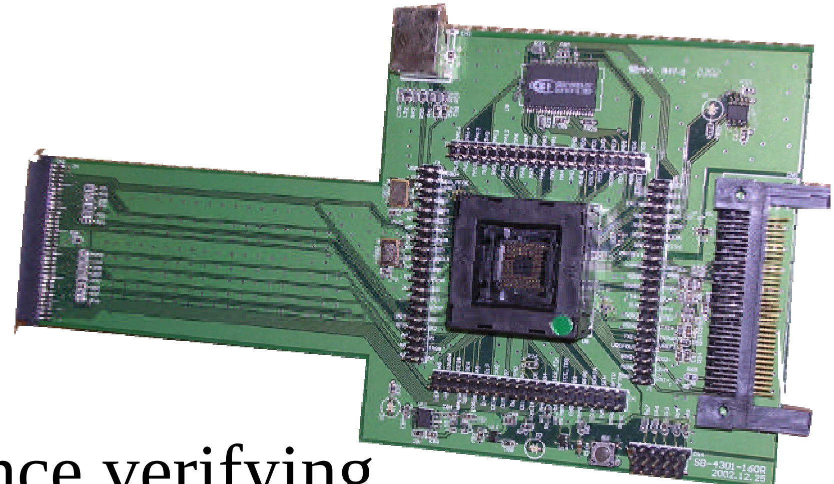
4. Verifying & Maintaining

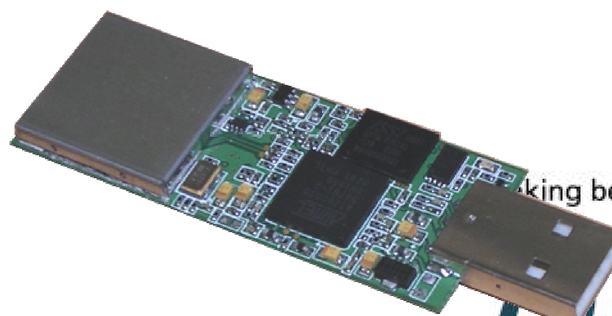
- Many Boards

  - Sorting Board : Sorting chips & Debugging





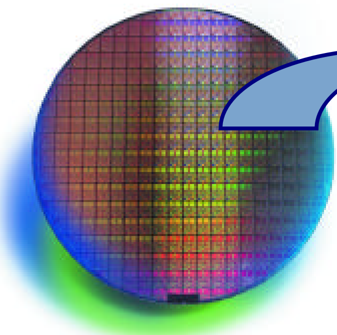
  - Demo Board : Performance verifying, Customer & Magazine Demo

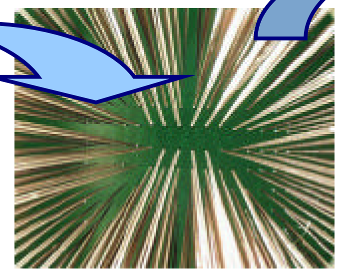


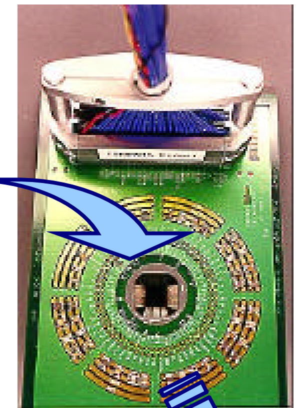
4. Verifying & Maintaining(cont.)

- Many Boards

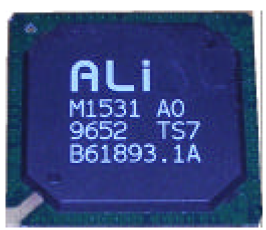
  - Probe Card : Chip probing on tester

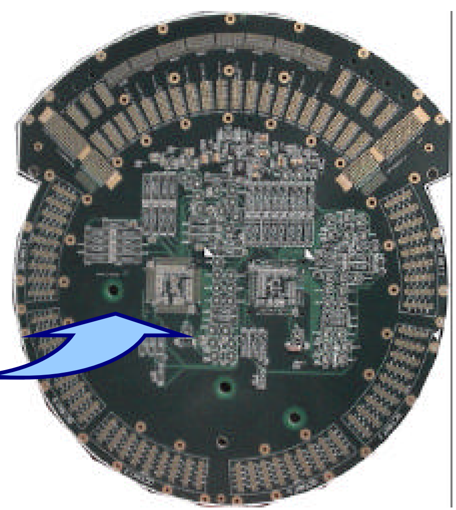






  - Load Board : Final test on tester

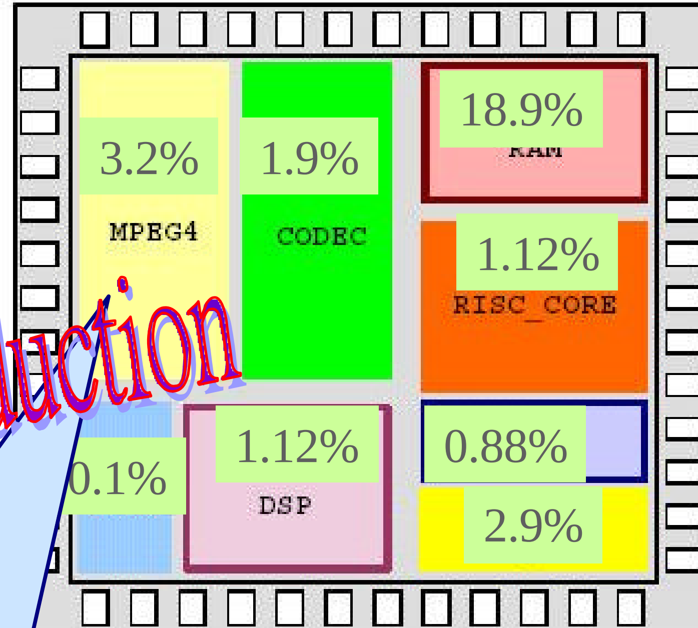




4. Verifying & Maintaining(cont.)

- Yield Rate Analysis

Statistics Result



Ready for Mass-Production

→Process Issue ?
→Design Quality Issue ?
→Testing Condition Issue ?
Shadow Pass / Over Constrain

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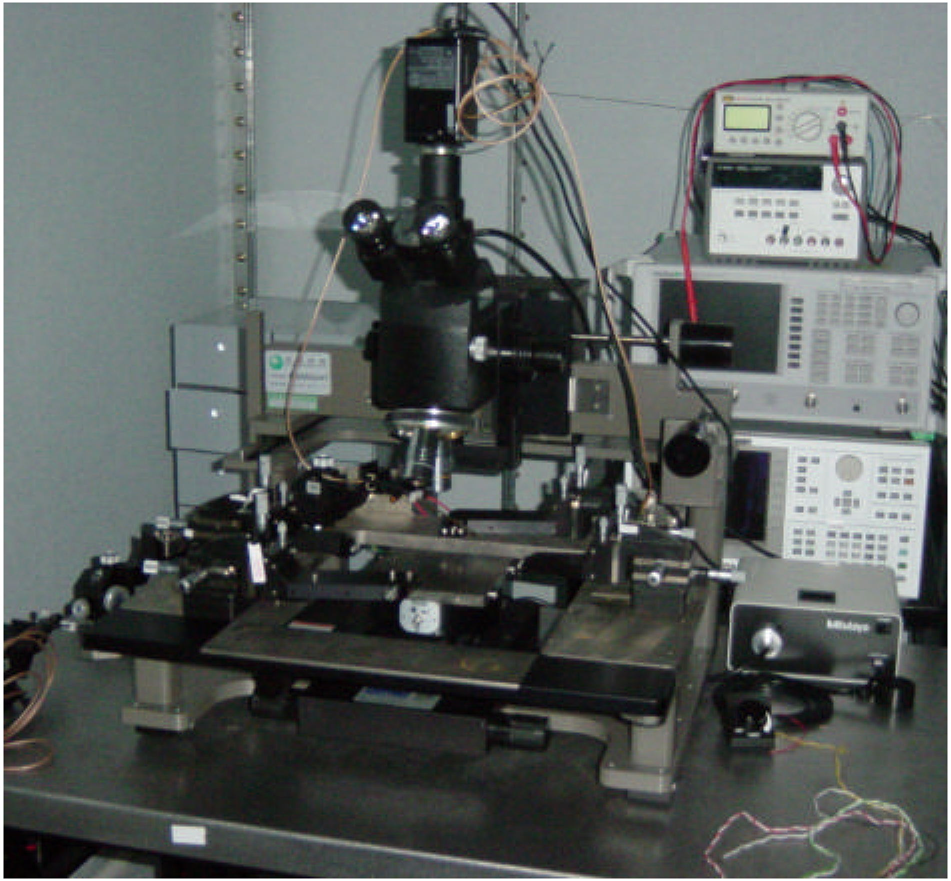
4. Verifying & Maintaining(cont.)

- Instruments for debugging, probing and measuring



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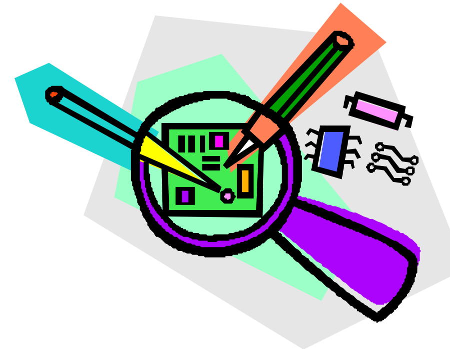
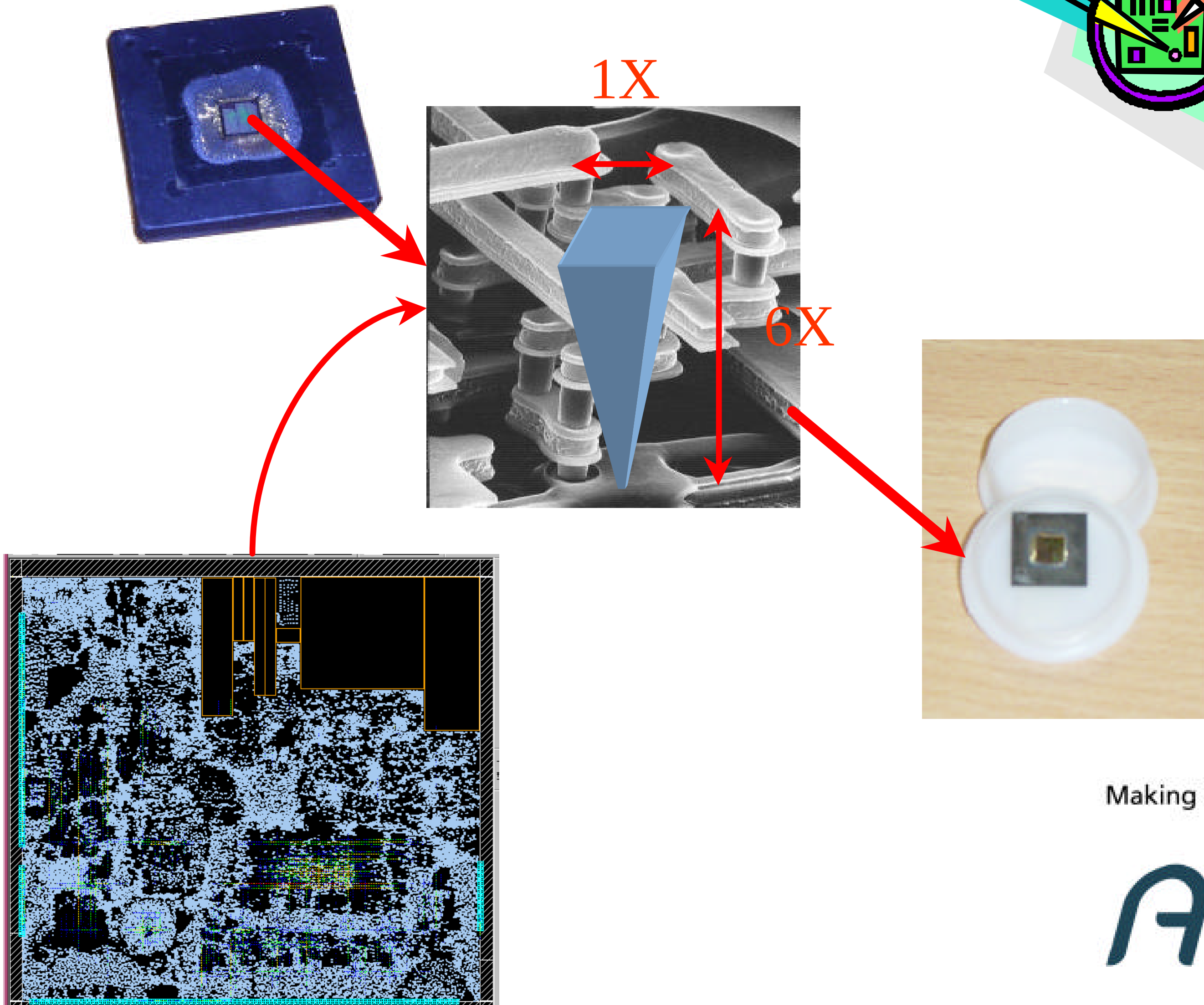
4. Verifying & Maintaining(cont.)

- FIB (Focused Ion Beam)





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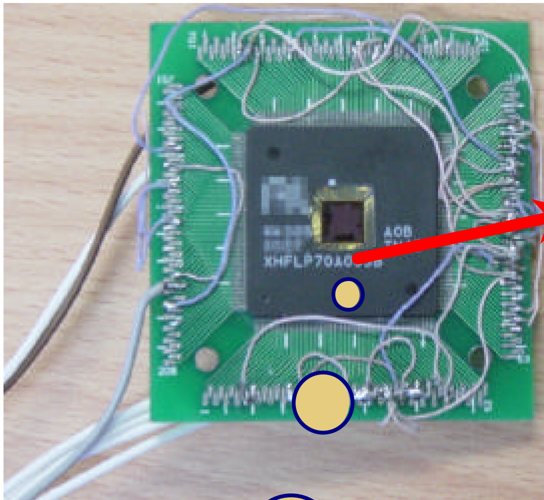
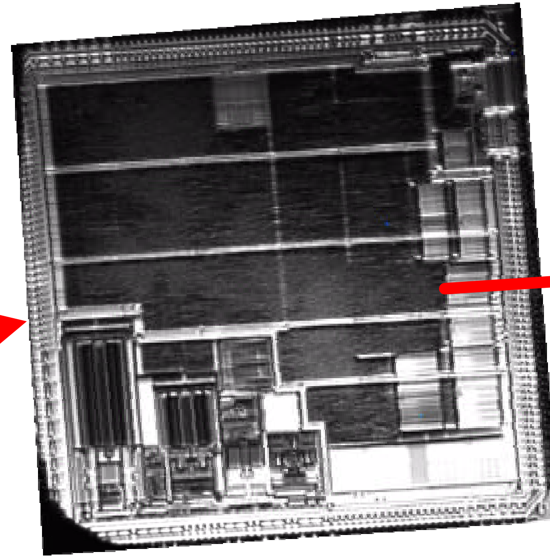
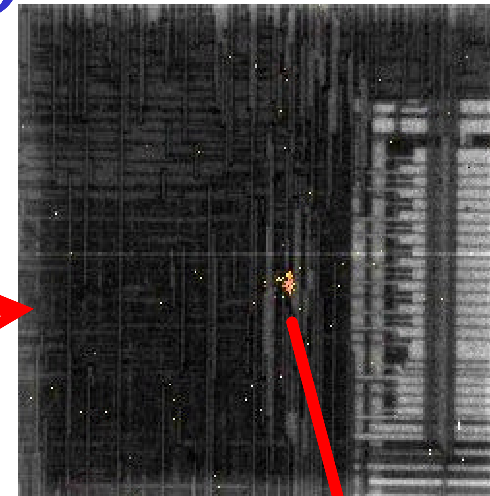
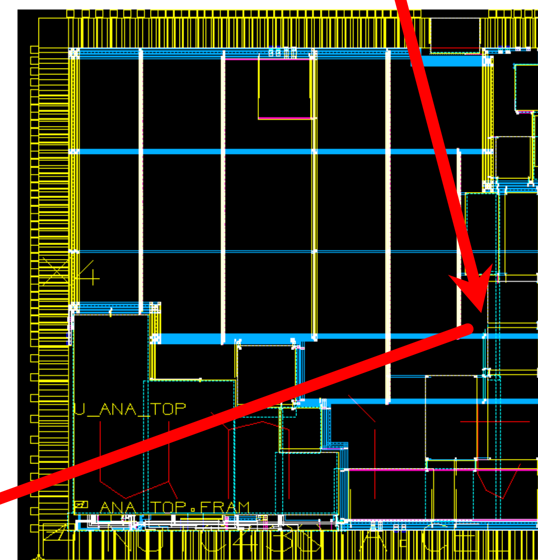
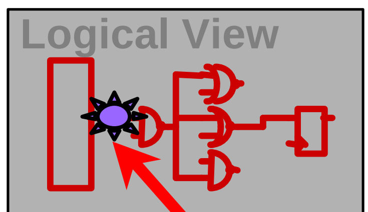
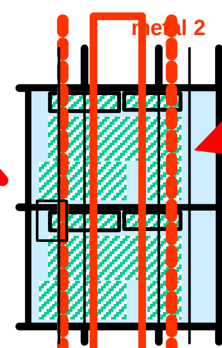
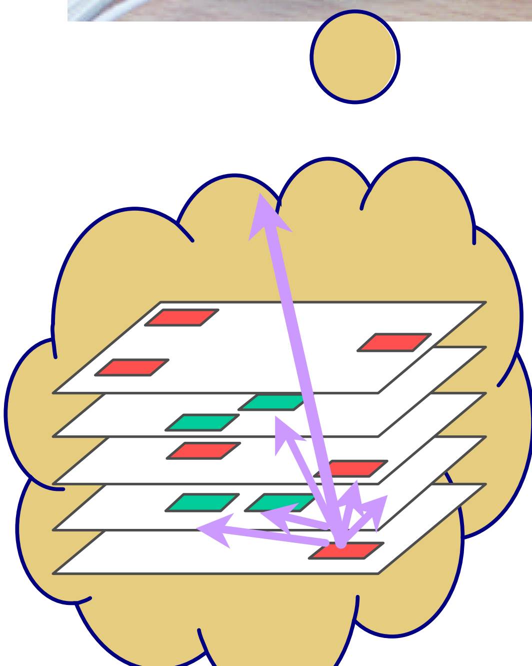
4. Verifying & Maintaining(cont.)

- EMMI

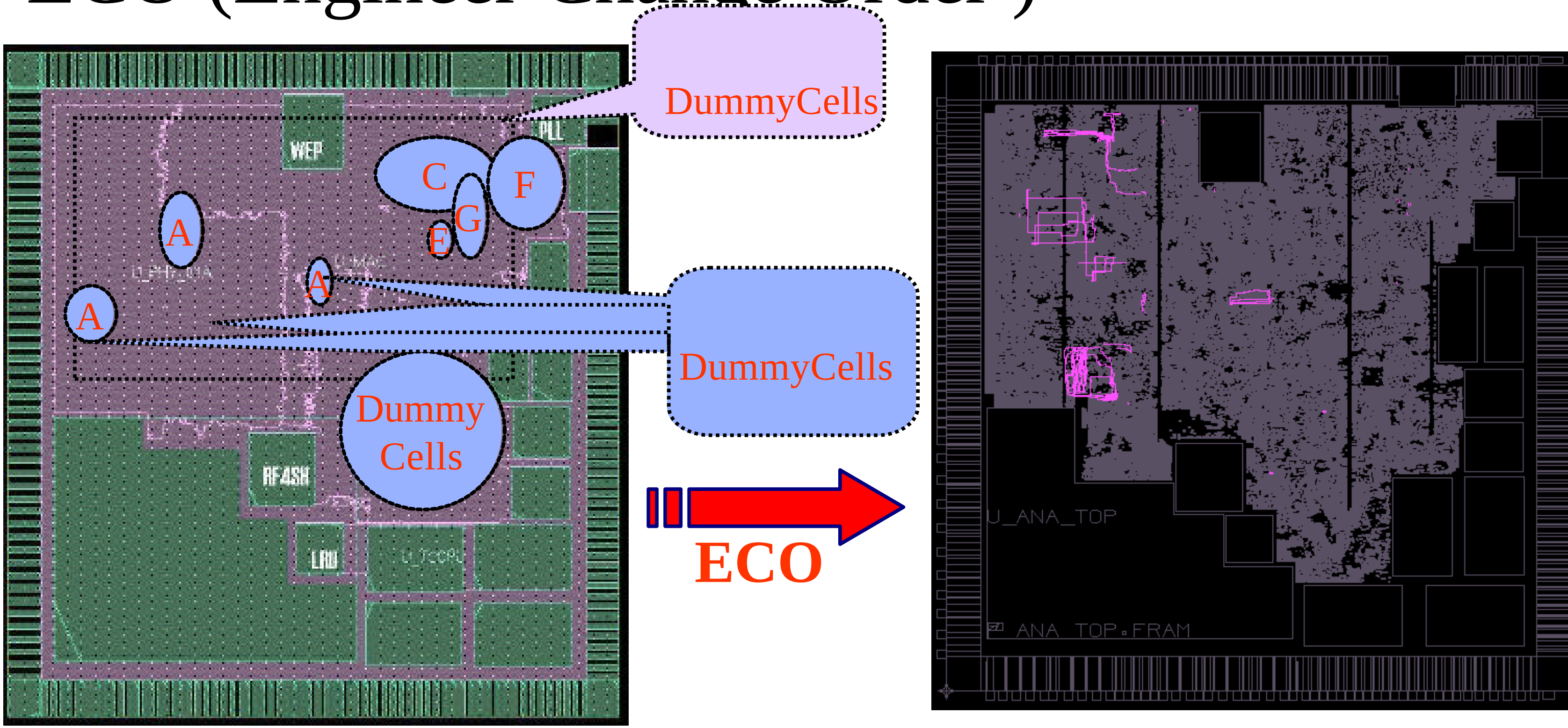






4. Verifying & Maintaining(cont.)

- ECO (Engineer Change Order)



- Customer Supporting

  - Design-In -> Design-Win -> Win-Win

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5. Conclusion

- Team-Work is basically essential.

製造者 : 柯國隆的爺爺柯貝博士

- Training yourself to be a --

  “high-EQ technical manager”.

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