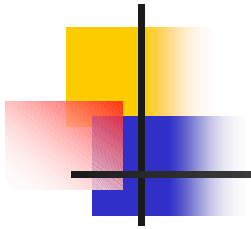
多媒體處理之超大型積體電路設計

國立中興大學電機工程學系

賴永康　博士



Outline

- Introduction
- JPEG, MPEG-1, MPEG-2, and MPEG-4
- Programmable Architectures
- Dedicated Architectures
- Conclusion

Introduction

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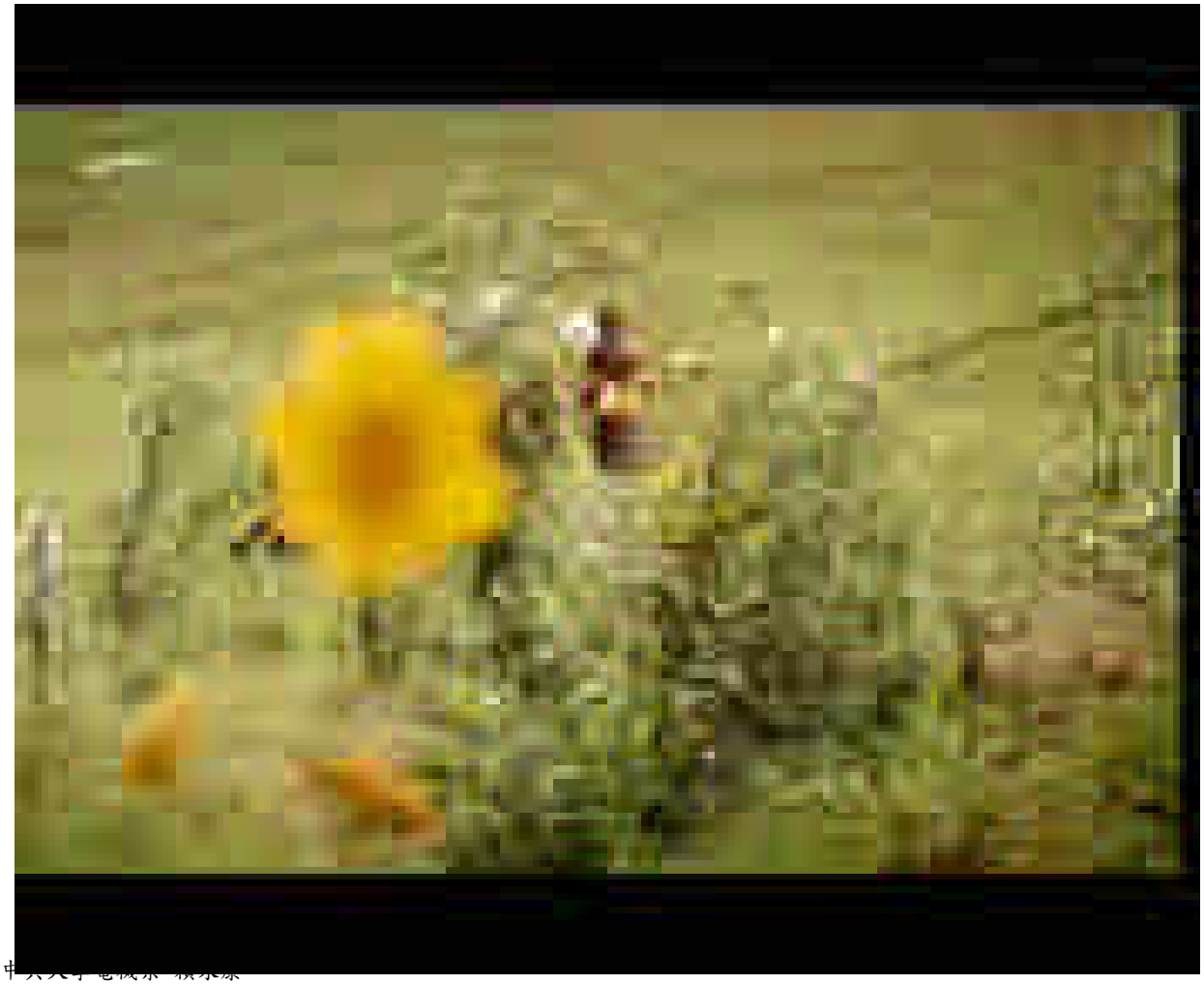

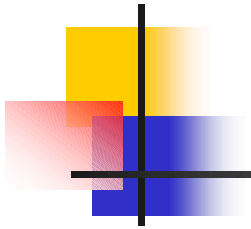

Introduction

- **Application Fields**
  - Image analysis (object recognition)
  - Image synthesis (X-ray tomography, synthetic aperture radar)
  - Video coding (JPEG, MPEG, H.263, Video Phone, and Video Conference)

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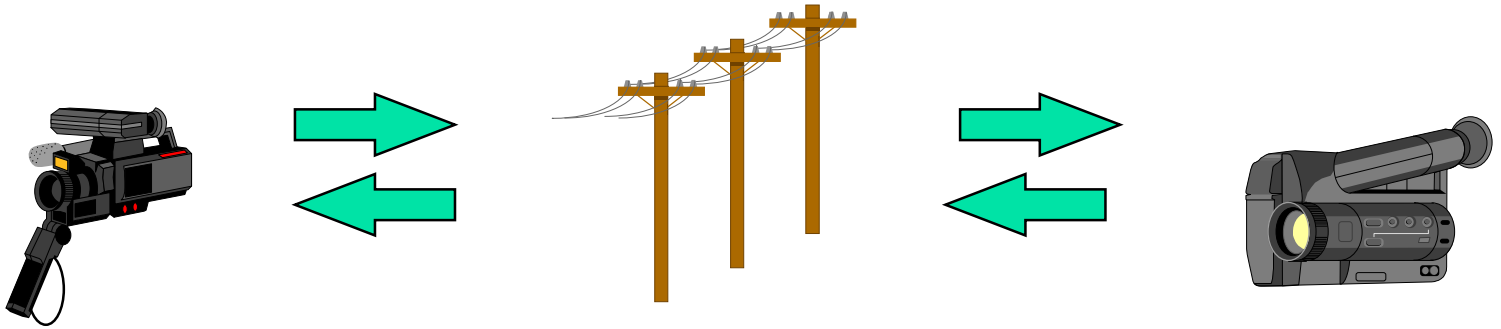
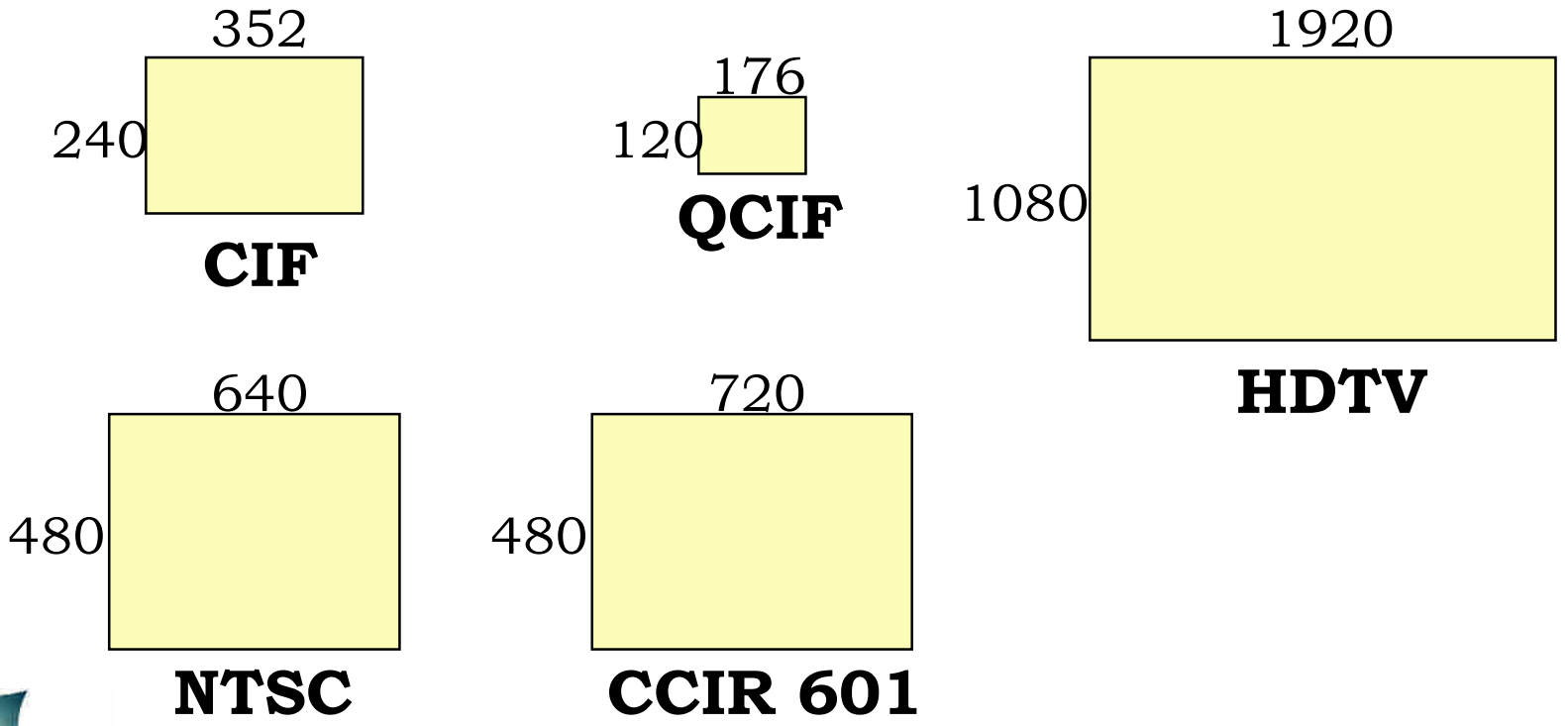
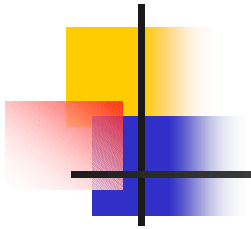
Video Conferencing System



- *Video equipments*
- *Audio equipment*
- *Network*
- *Window Interface*

Digital Video Format



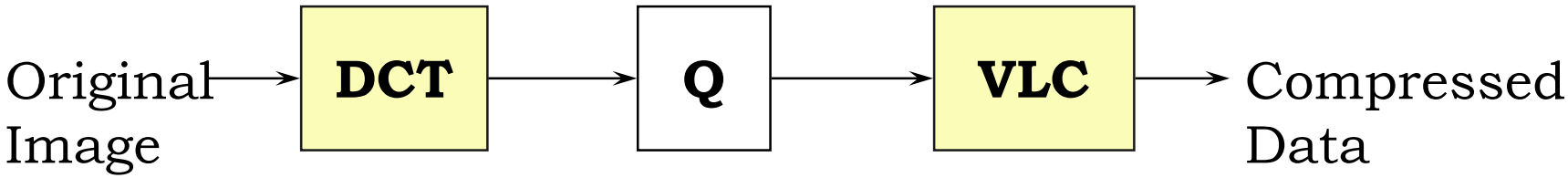


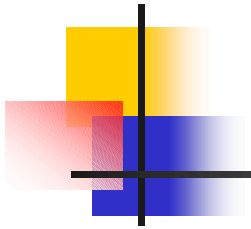
Digital Video Format (cont.)

Format	Data Amount	Bit-Rate
352x240 CIF	30.4 Mbits/s	1.5 Mbits/s
720x480 CCIR 601	165.9 Mbits/s	15-25 Mbits/s
1920x1080 HDTV	1.9 Gbits/s	80 Mbits/s

ISO/IEC JPEG

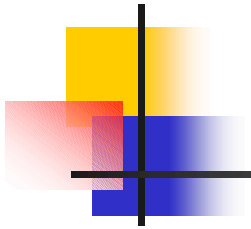
- Still image compression
- DCT, RLC, VLC, Predictive DC
- Loss compression
- Compression ratio 8 ~ 10





ISO/IEC MPEG-1

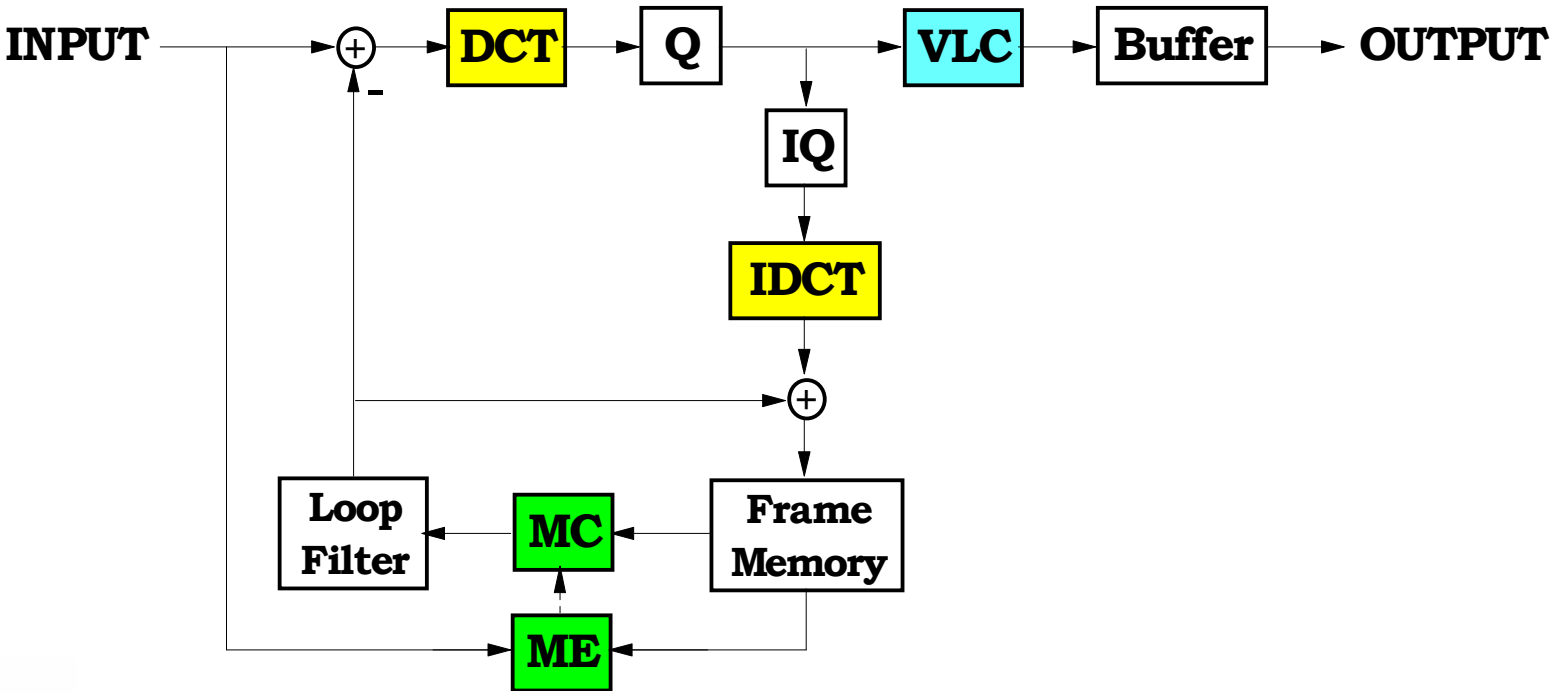
- Media storage
- Optimal for frame size 352x240x30 or 352x288x25
- Bitrate: up to 1.5 Mbit/s
- International standard in 1992
- Single chip for the whole system



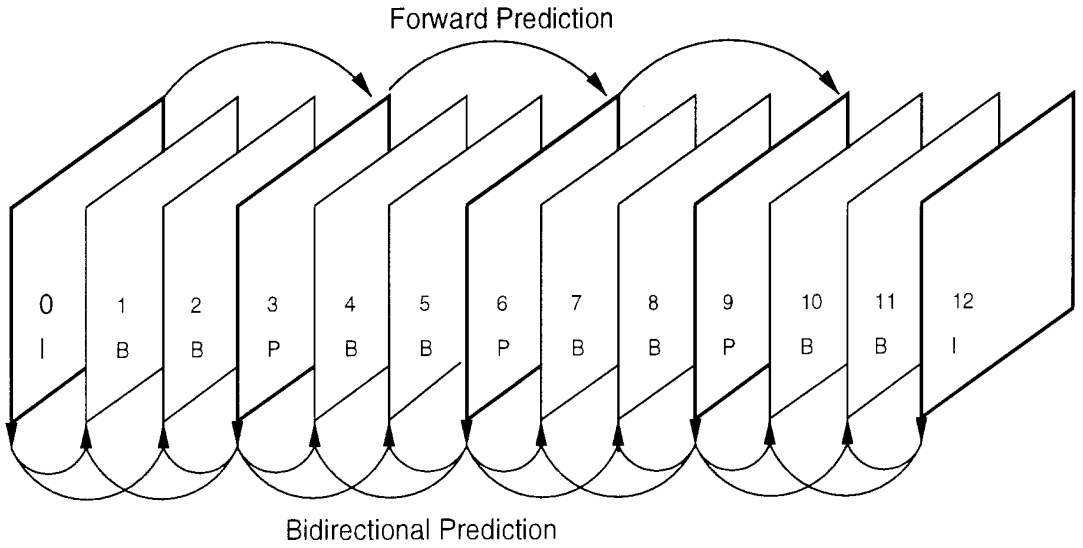
ISO/IEC MPEG-2

- Applications from storage to HDTV
- Bitrate: standard definition TV: 4-9 Mbit/s
  HDTV: 15-25 Mbit/s
- Interlaced/non-interlaced
- Scalability
- Capable of decoding MPEG-1 bitstream
- International standard in 1994
- Single chip for video and audio

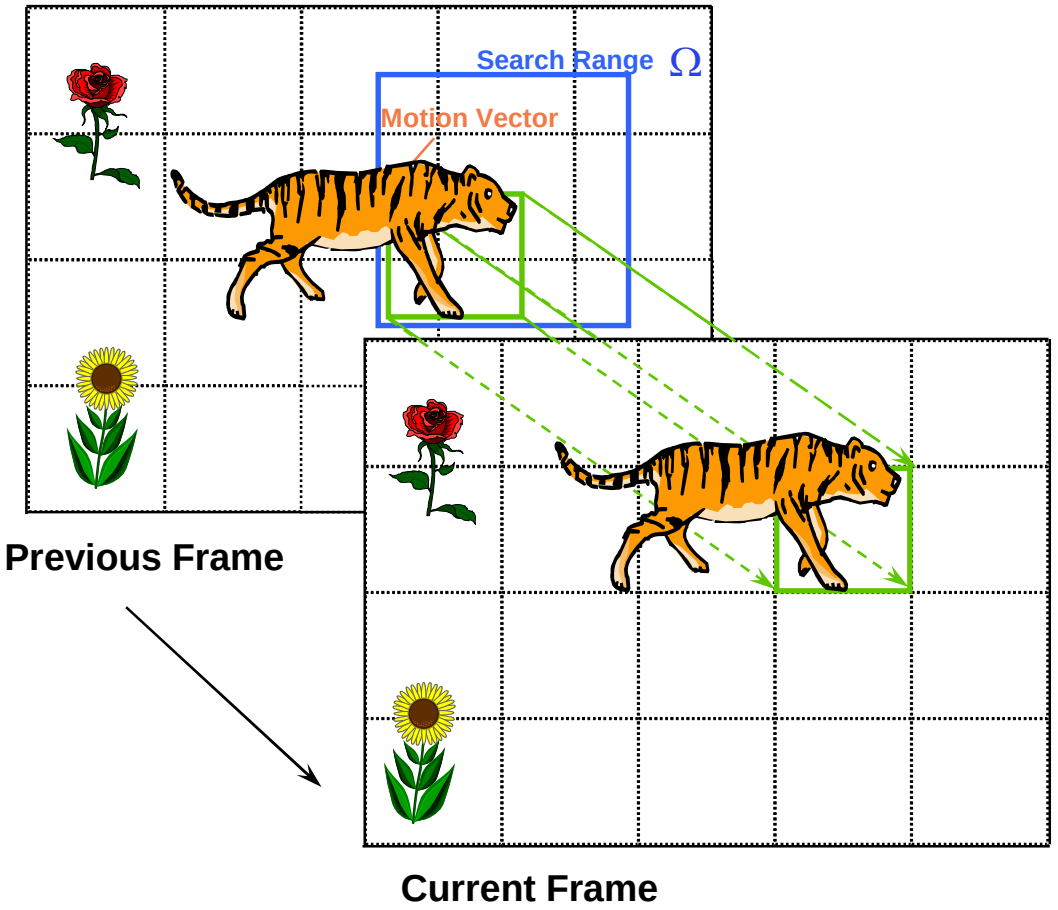
ISO/IEC MPEG


INPUT
DCT
Q
VLC
Buffer
OUTPUT
IQ
IDCT
Loop Filter
MC
Frame Memory
ME

Video Sequence



Motion Compensation/Estimation



Motion Compensation/Estimation

Original

Reconstructed

Difference

Discrete Cosine Transform

- Block size: 8 x 8
- Two-dimensional DCT:

$$F(u,v) = \frac{2}{N} C(u)C(v) \sum_{u=0}^{N-1} \sum_{v=0}^{N-1} f(x,y) \cos\frac{2\pi(2x+1)u}{4N} \cos\frac{2\pi(2y+1)v}{4N}$$

$$C(u), C(v) = \begin{cases} 1/\sqrt{2}, & u,v = 0 \\ 1, & \text{otherwise} \end{cases}$$

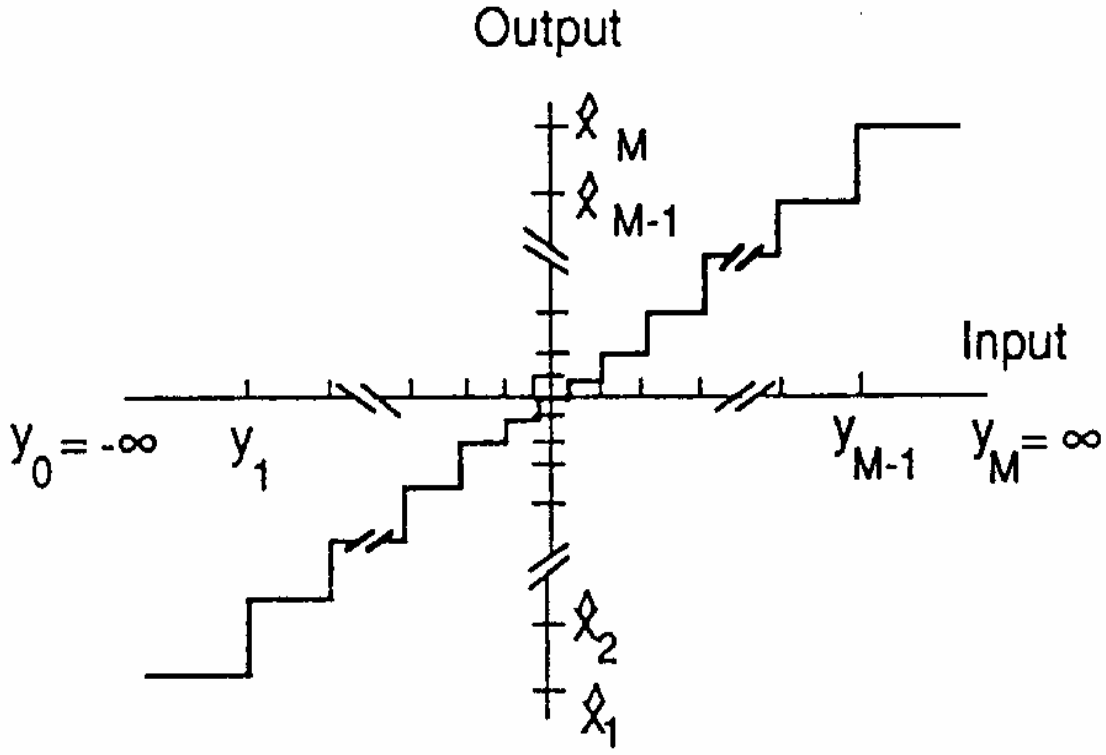
Separable -- row-column method

- Most large coefficients concentrate on the upper-left corner
- Quantization and zig-zag scan

Discrete Cosine Transform

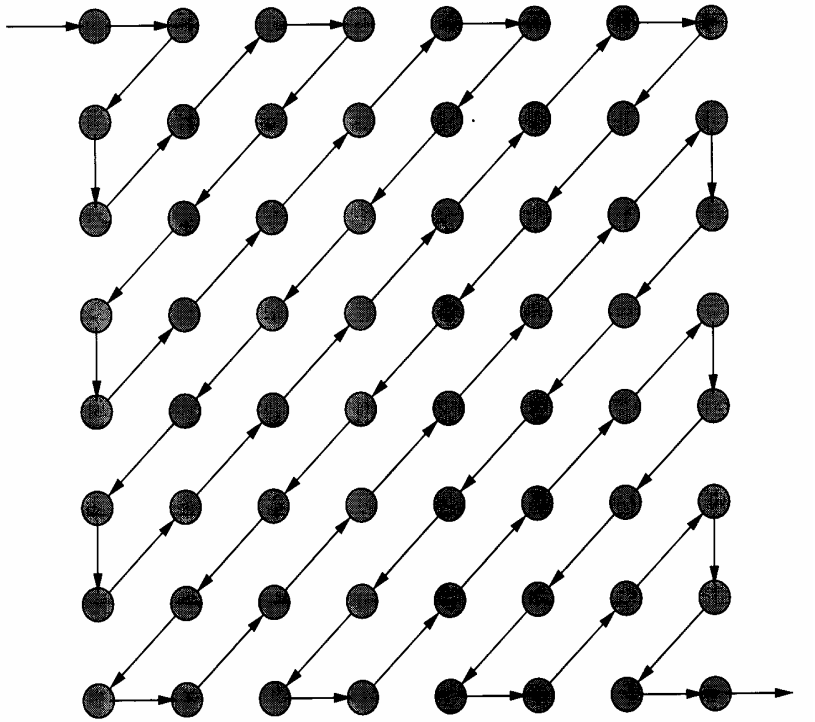
Quantization

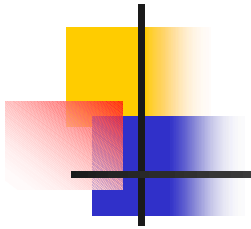
- Each of 64 DCT coefficients is then quantized.



Zig-Zag Scanning

- DCT coefficients are coded in Zig-Zag scanning process.





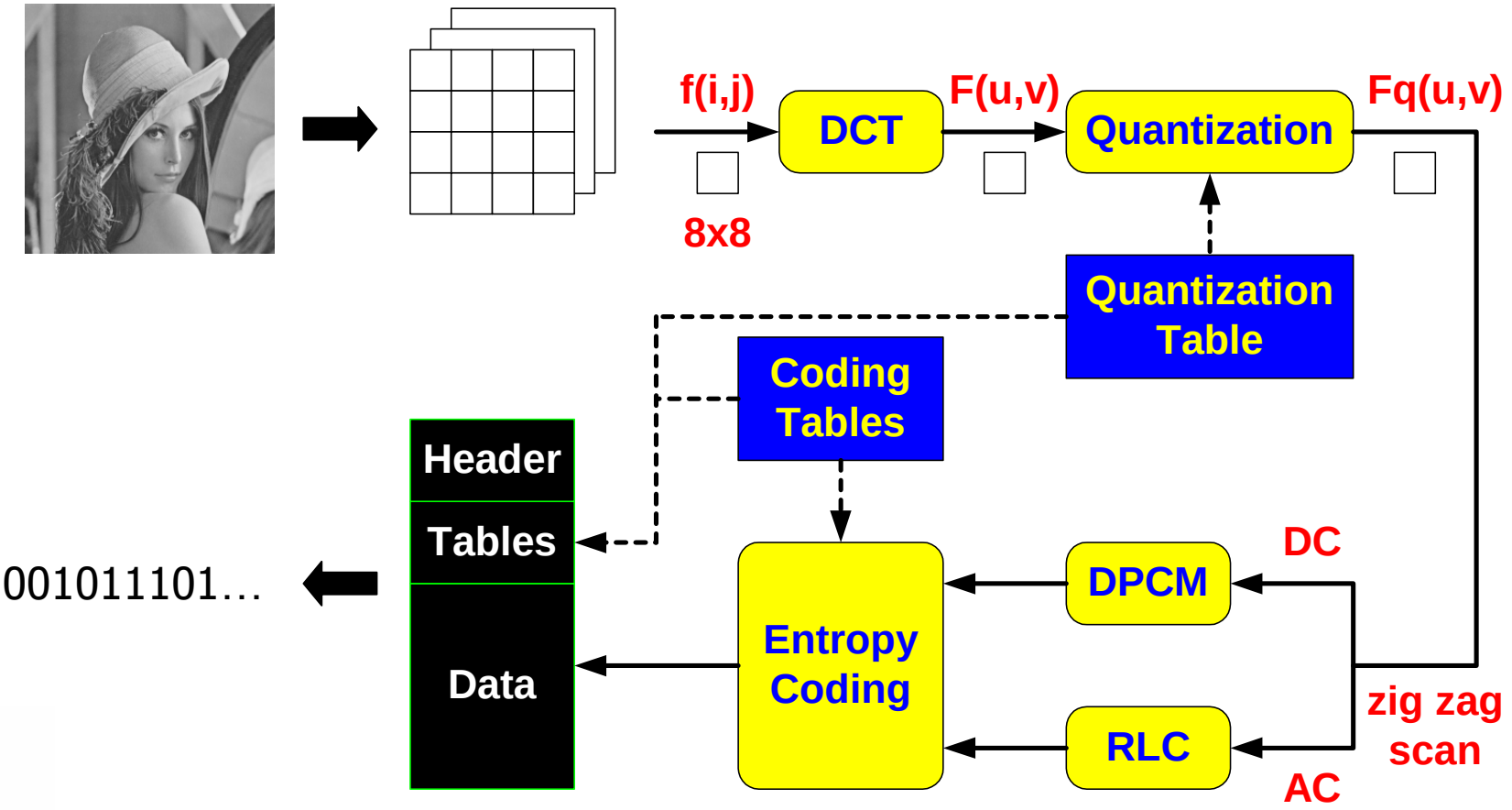
Variable Length Coding

- To reduce the statistical redundancy
- Probability-based codewords arrangement
- Huffman Coding

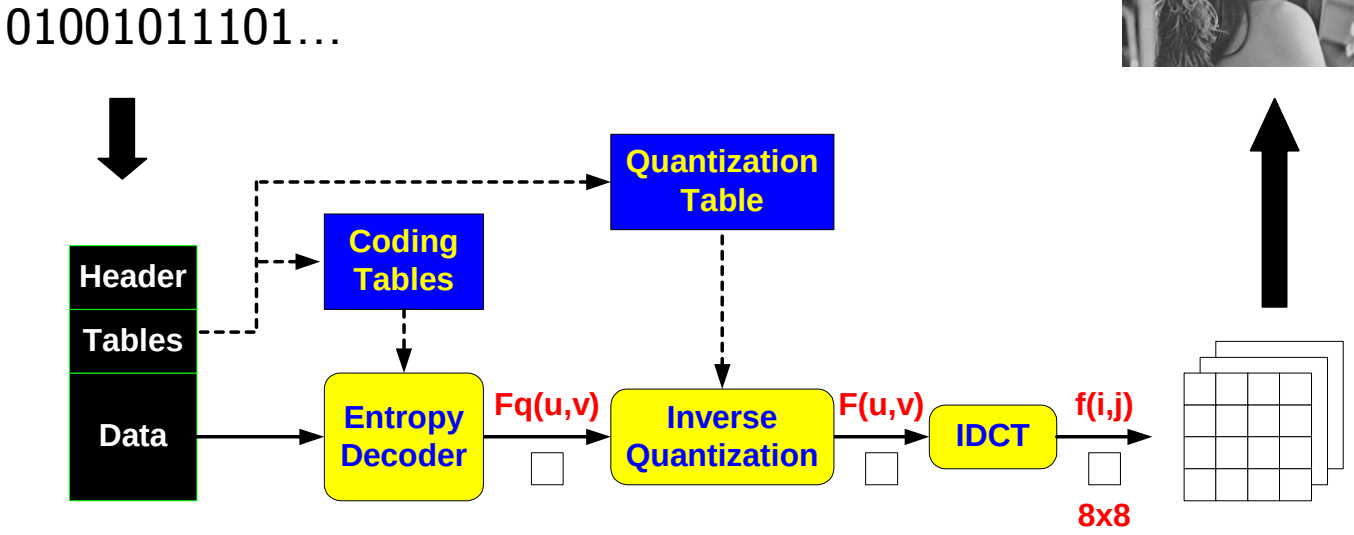
S1	0.45	1
S2	0.3	00
S3	0.15	010
S4	0.1	011

  - S4 S1 S2 S2 S3 S1 <---> 011100000101
- Arithmetic coding

Block Diagram of JPEG Encoder

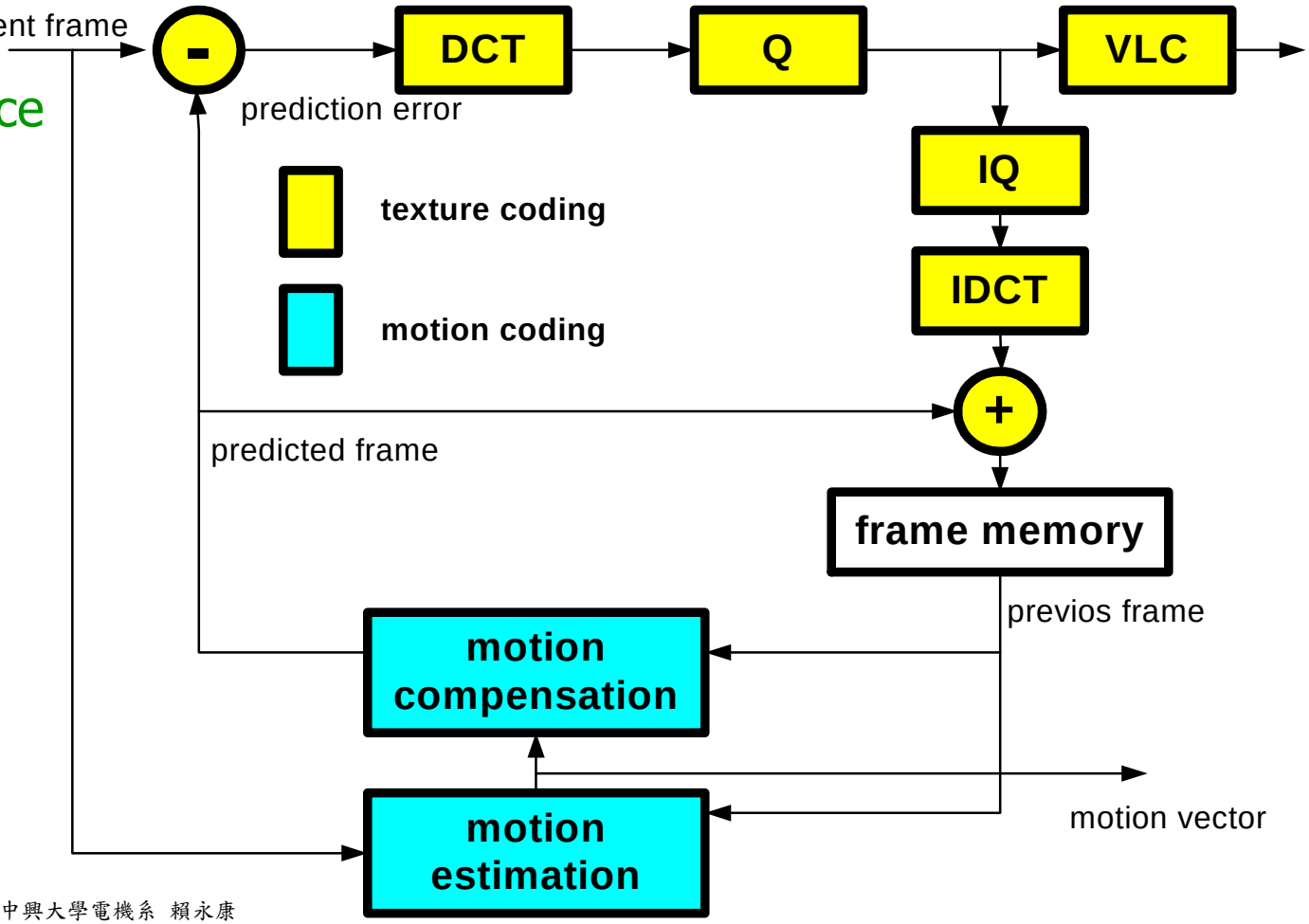


Block Diagram of JPEG Decoder

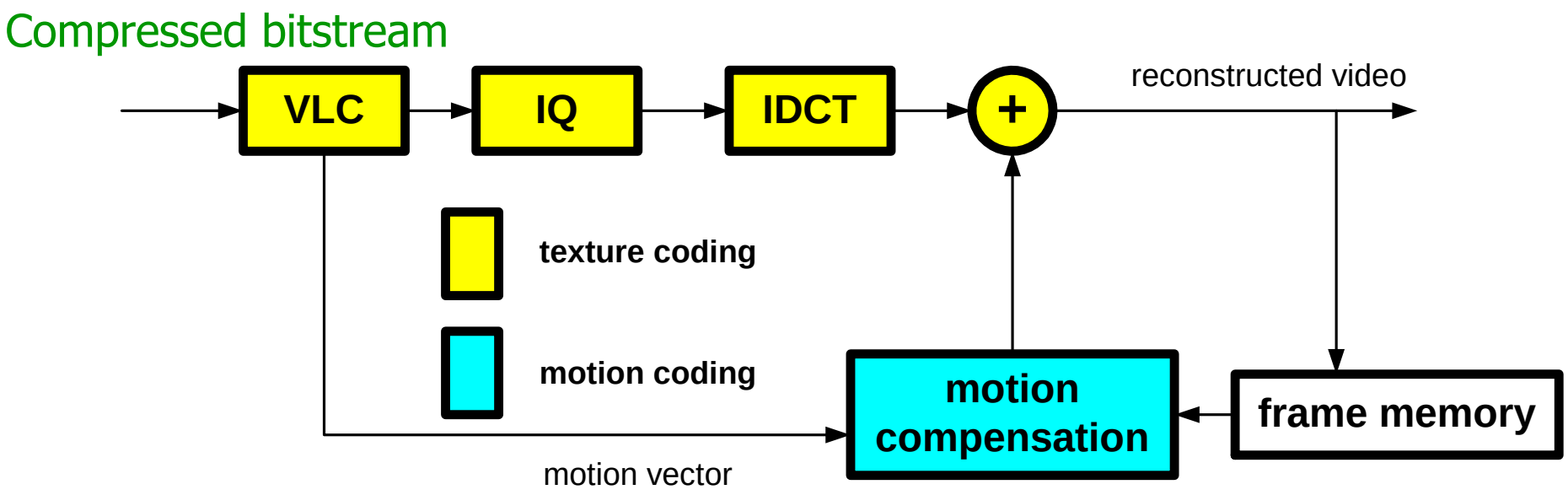


MPEG video encoder

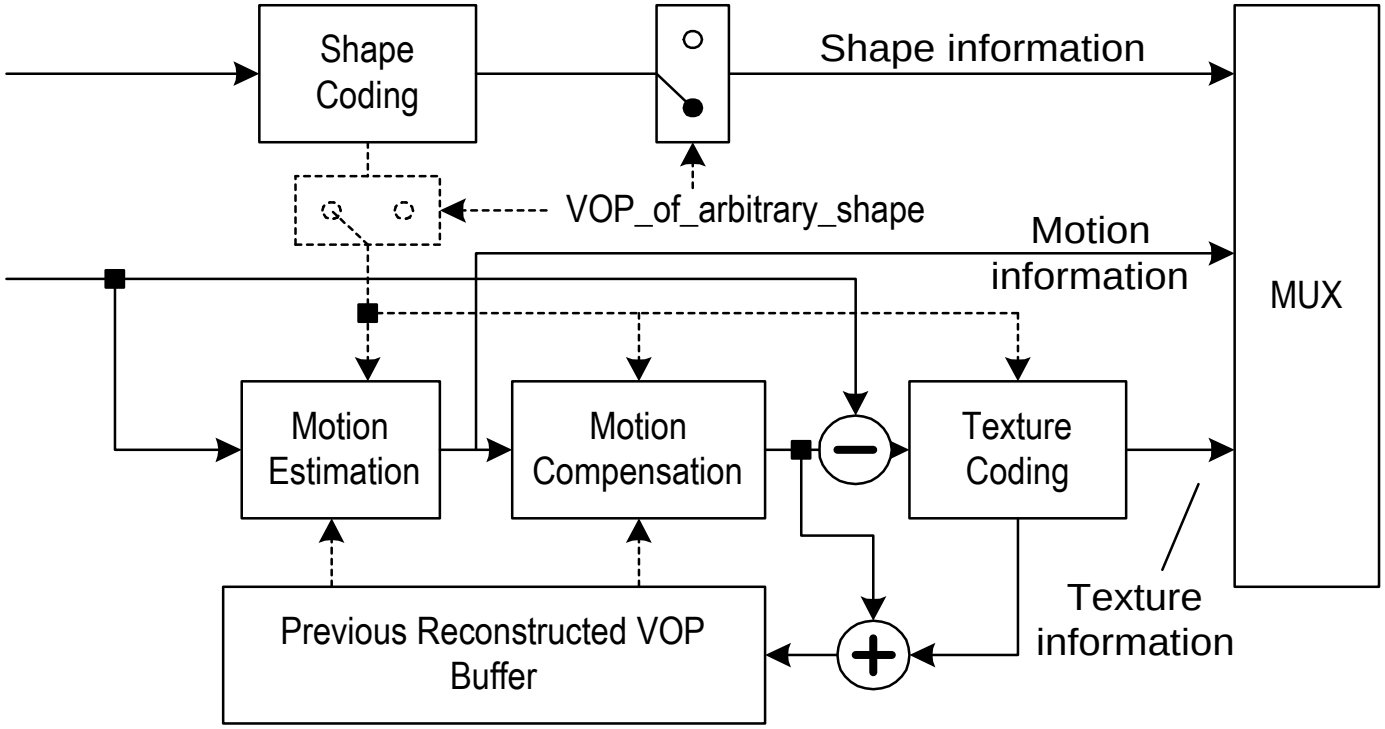
Video sequence



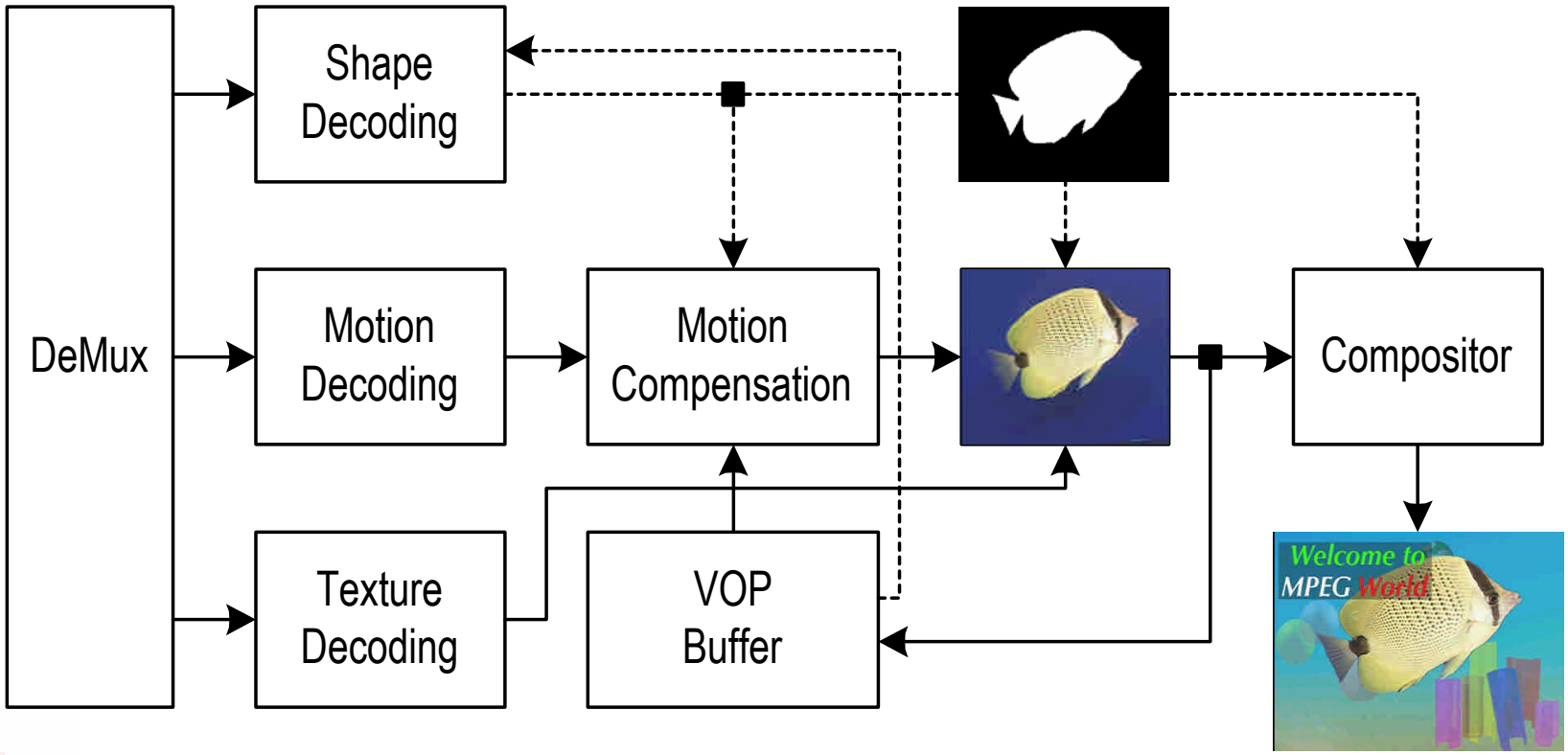
MPEG video decoder

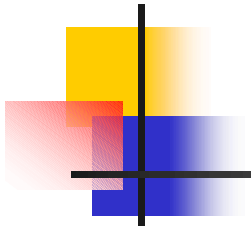


MPEG-4 Video Encoding



MPEG-4 Video Decoding





Difficulties in Realization

- Large amount of image/video data
- Real-time processing requirement
- Several thousand megaoperations per second

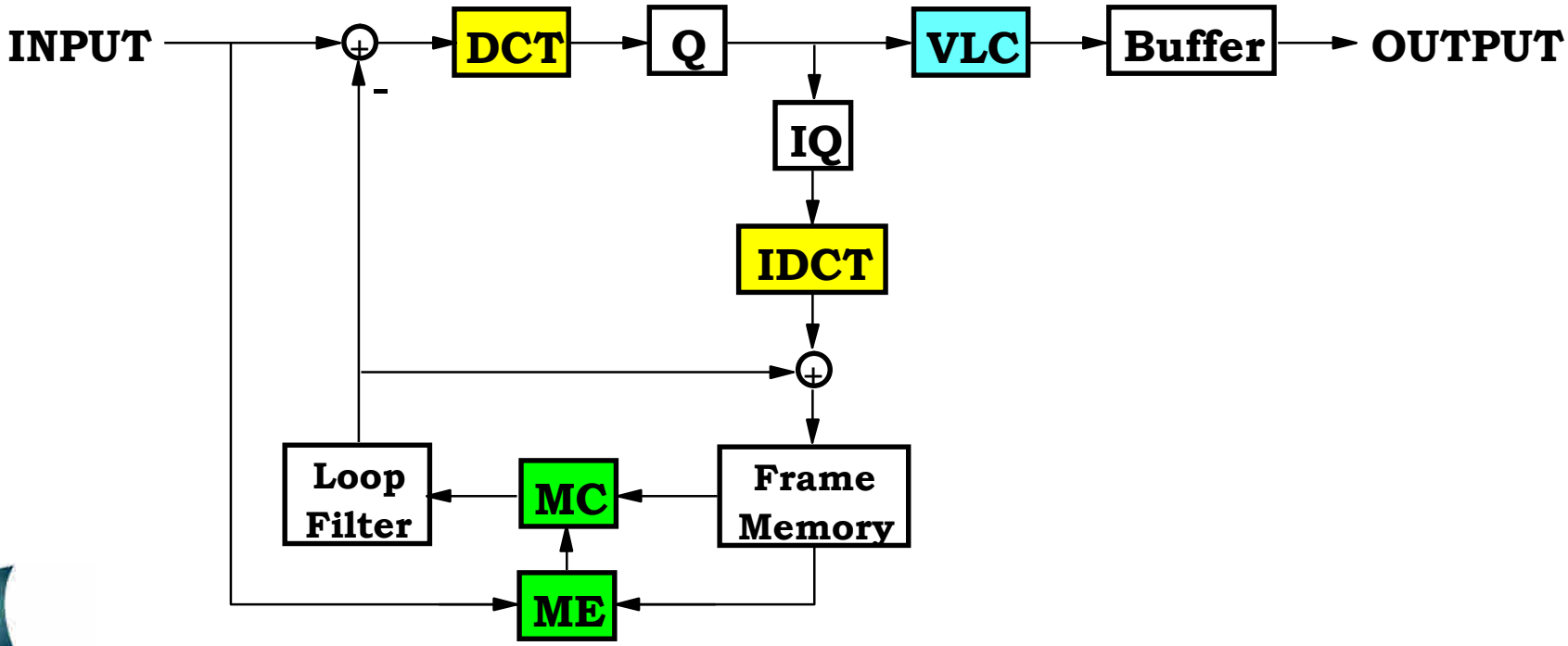
- Software Solution
- Hardware Solution (VLSI)

Approaches to VLSI Implementation

- **Programmable Architecture**
  - Cover wide range of different algorithms
  - Simple software modifications for the change of algorithms
  - Rapid prototyping
- **Dedicated Architecture**
  - Matched to one application
  - High processing power and compact implementation
  - Inflexibility for subsequent changes in algorithms

A Typical Video Compression System

- Video coding (JPEG, MPEG, H.263, Video Phone, and Video Conference)



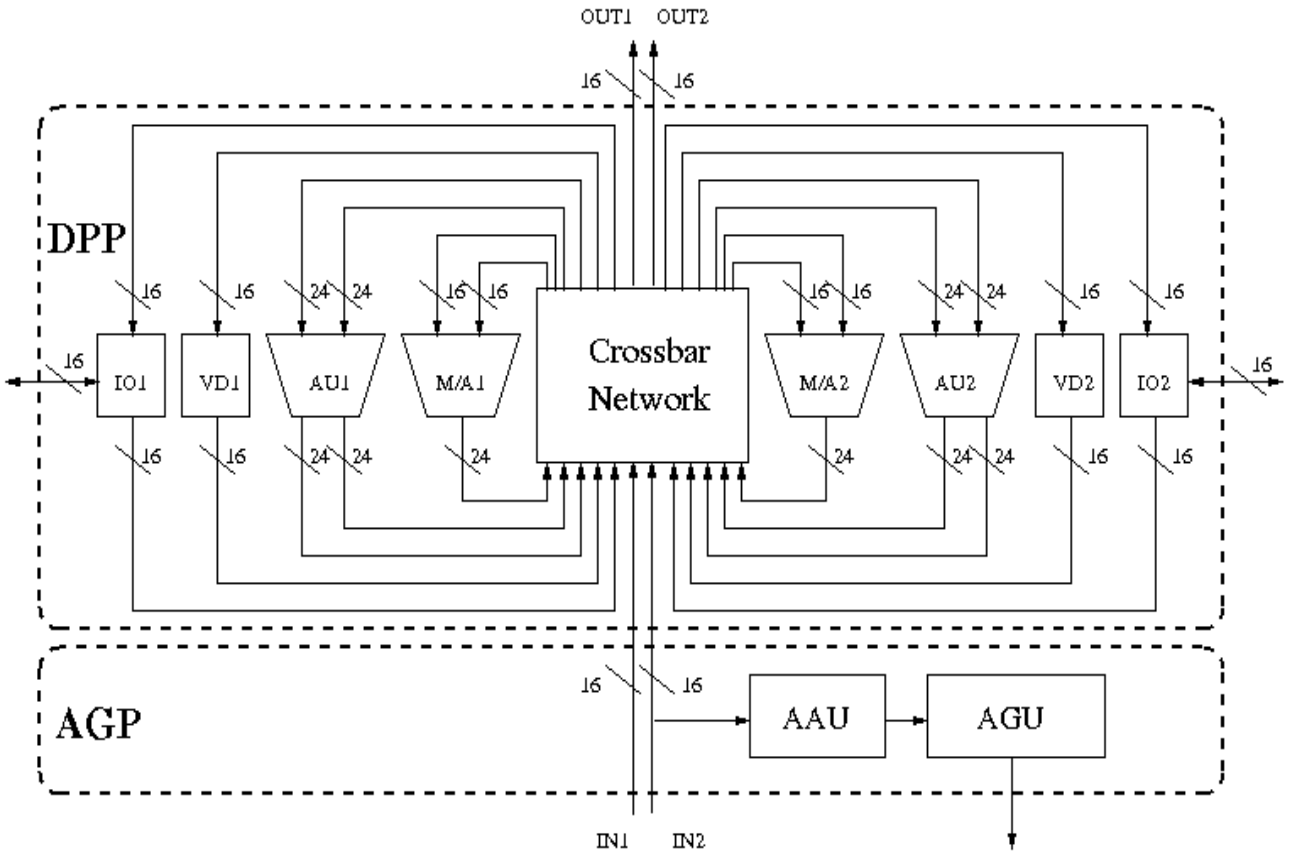
Typical Video Signal Processing

TYPICAL VIDEO SIGNAL PROCESSING

Processing	Operation	Addressing
Motion Estimation	$\Sigma\|x-y\|$ or $\Sigma(x-y)^2$	2-D block (Sliding)
Transform Coding	$\Sigma a \times x$	2-D block
Vector Quantization	$\Sigma a \times x$ or $\Sigma(x-y)^2$	2-D block
Convolution	$\Sigma x \times y$	2-D block (Sliding)
Filtering	$a \times x + b$	2-D block
FFT	$a \times x + b$	Bit Reverse

VSP Architecture with Reconfigurable Pipelined Architecture

- Block Diagram



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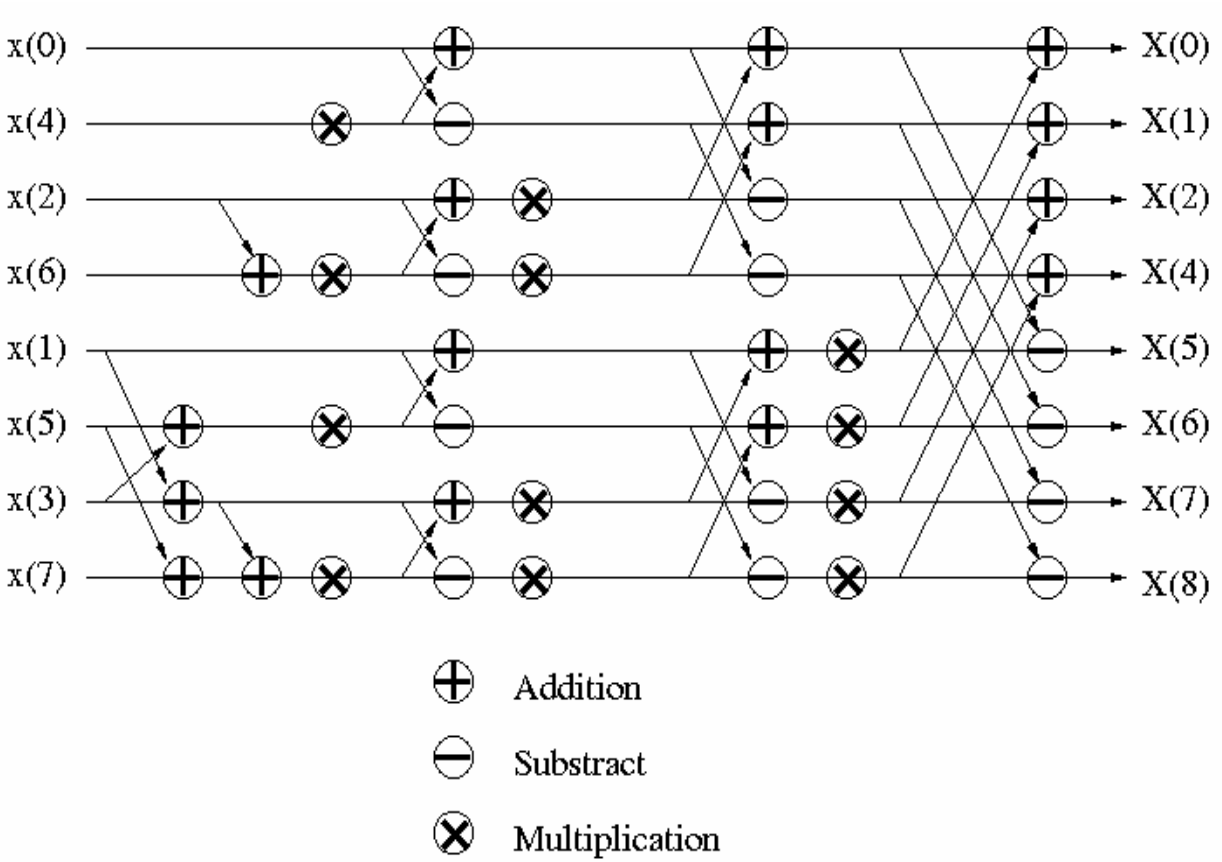
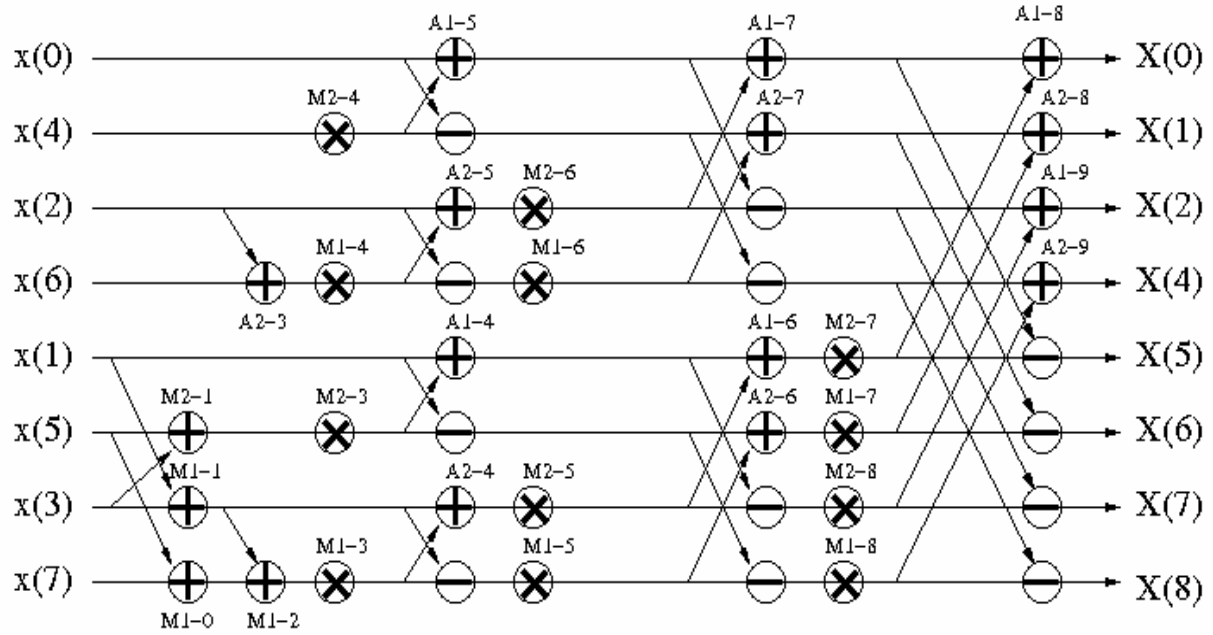
Performance Analysis

- Lee's Algorithm (FDCT) , 1984



Performance Analysis (cont.)



M1–4: M/A1 at clock 4

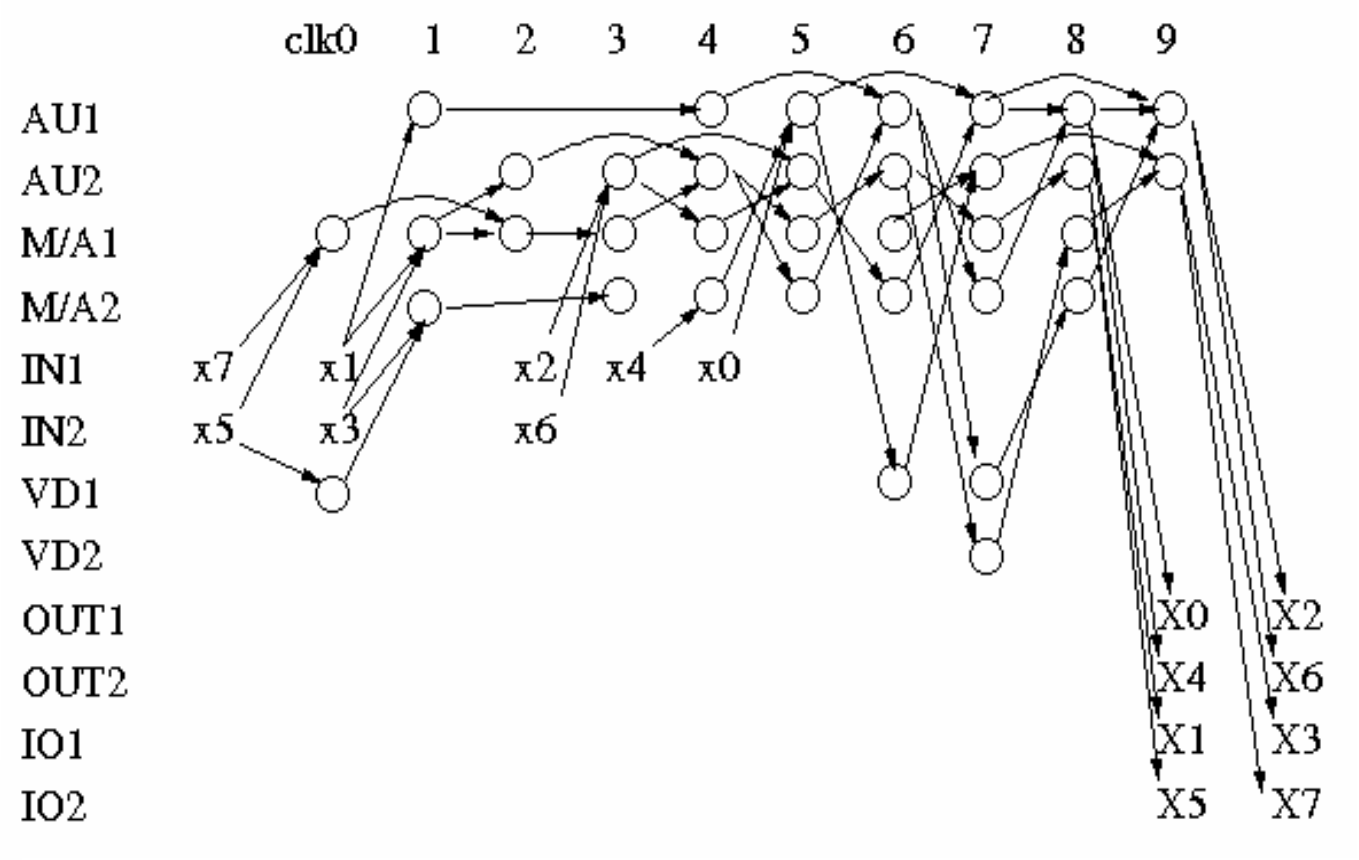
A2–5: AU2 at clock 5

⊕ Addition

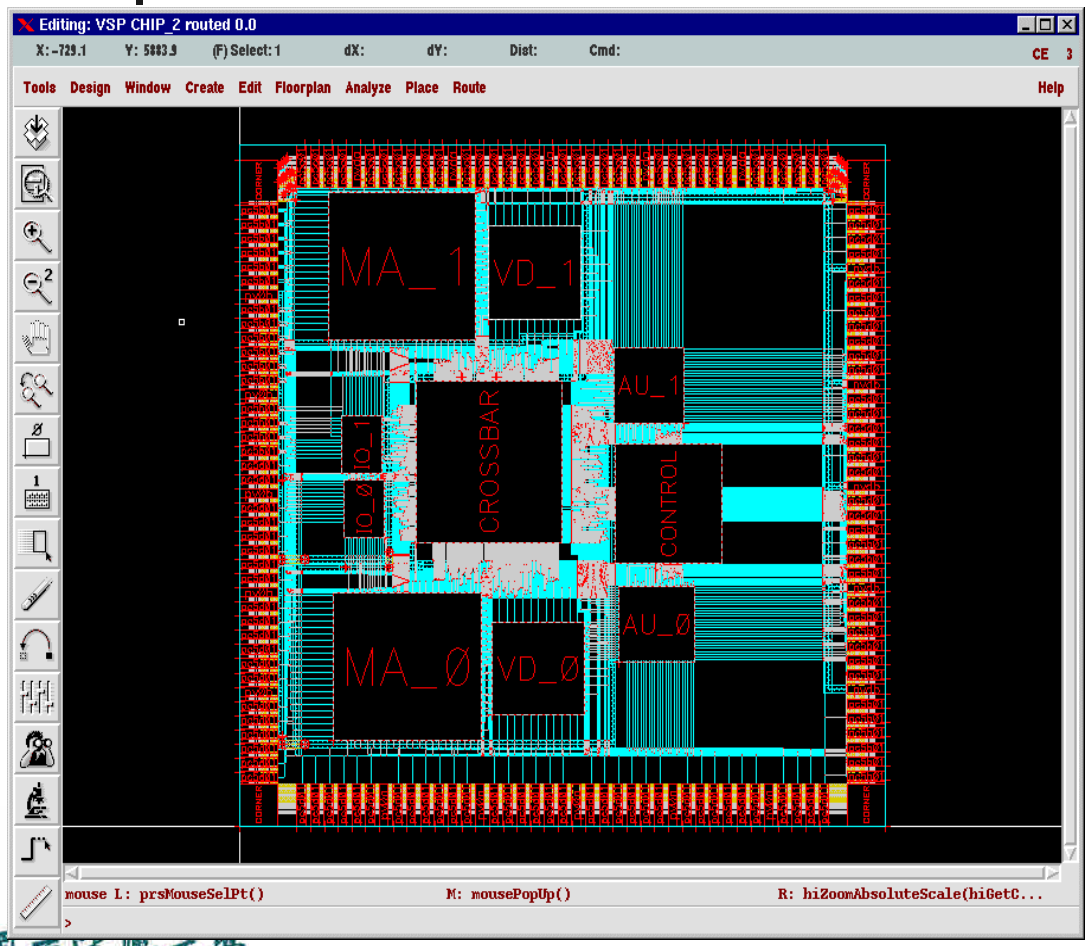
⊖ Substract

⊗ Multiplication

Performance Analysis (cont.)



Chip Layout



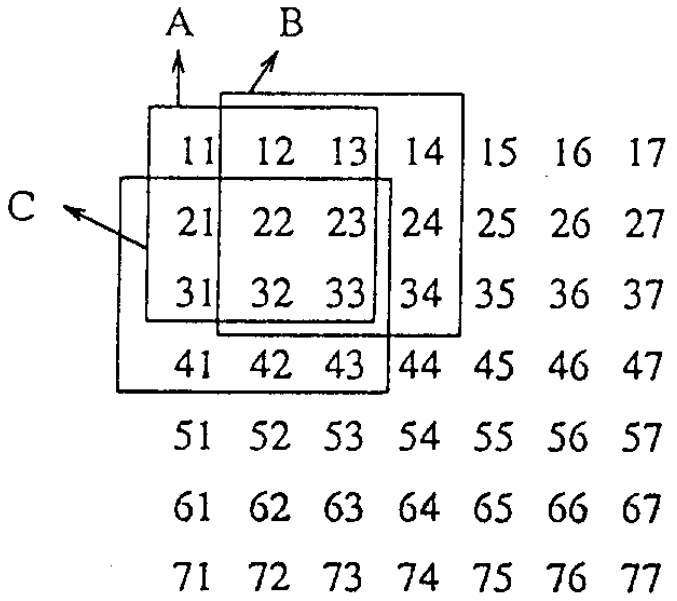
Technology	COMPASS 0.6 µm CMOS
Die Size	7.9 mm * 8.1 mm
Number of Transistors	31128
Number of Pins	159 pins
Instruction Cycle	40 ns
Performance	150 MOPS

Block-Matching Criteria

- Current block candidate bl

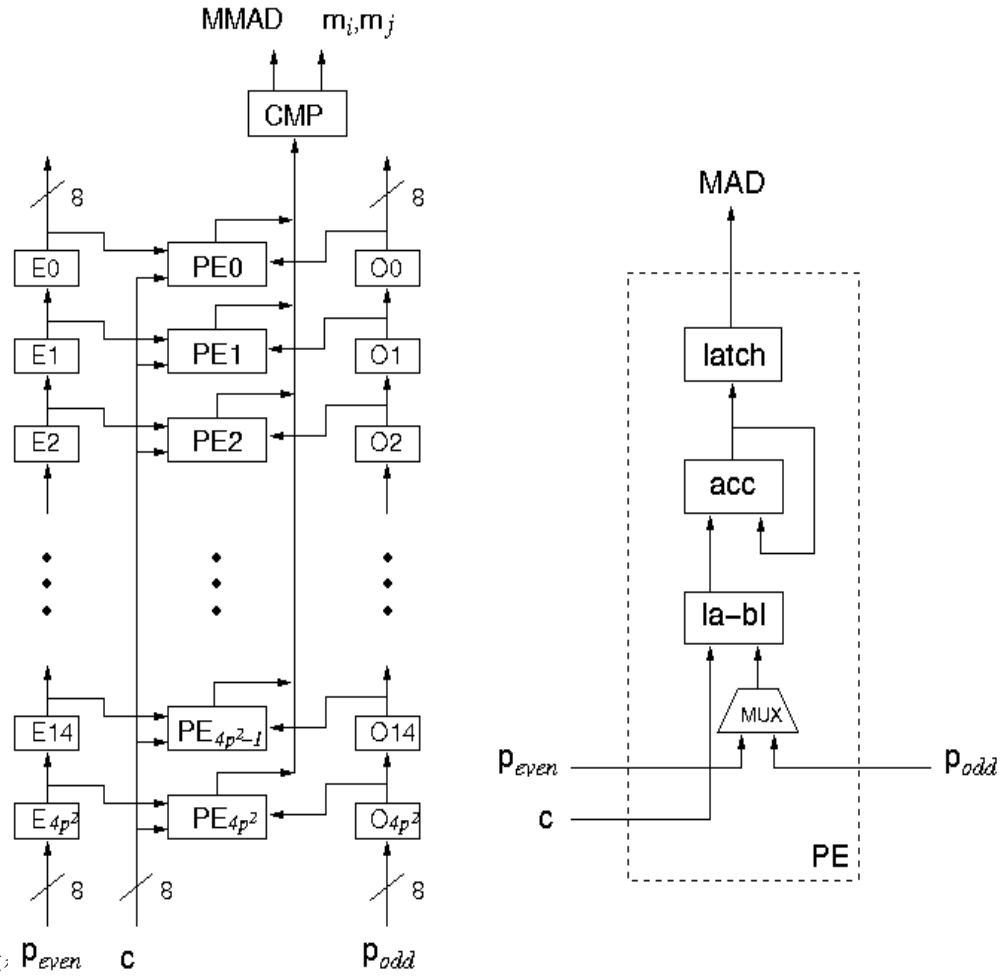
A	B	C
D	E	F
G	H	I

a	b	C
d	e	f
g	h	i



$$MAD(i,j) = MAD(i,j) + |X(k,l)-Y(k+i,l+j)|$$

Motion Estimation Processor for Full Search Block-Matching Algorithm

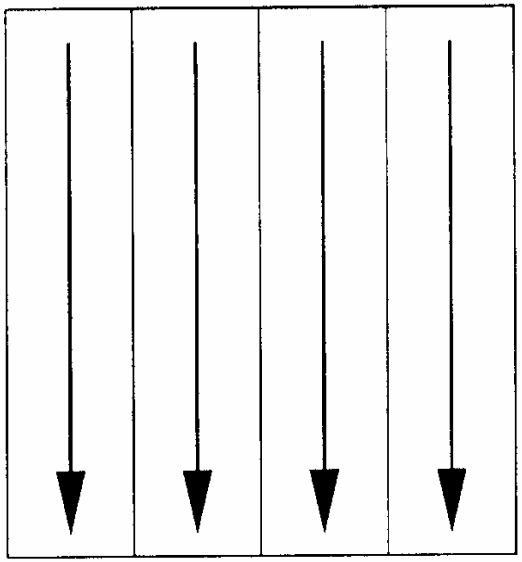


An Example

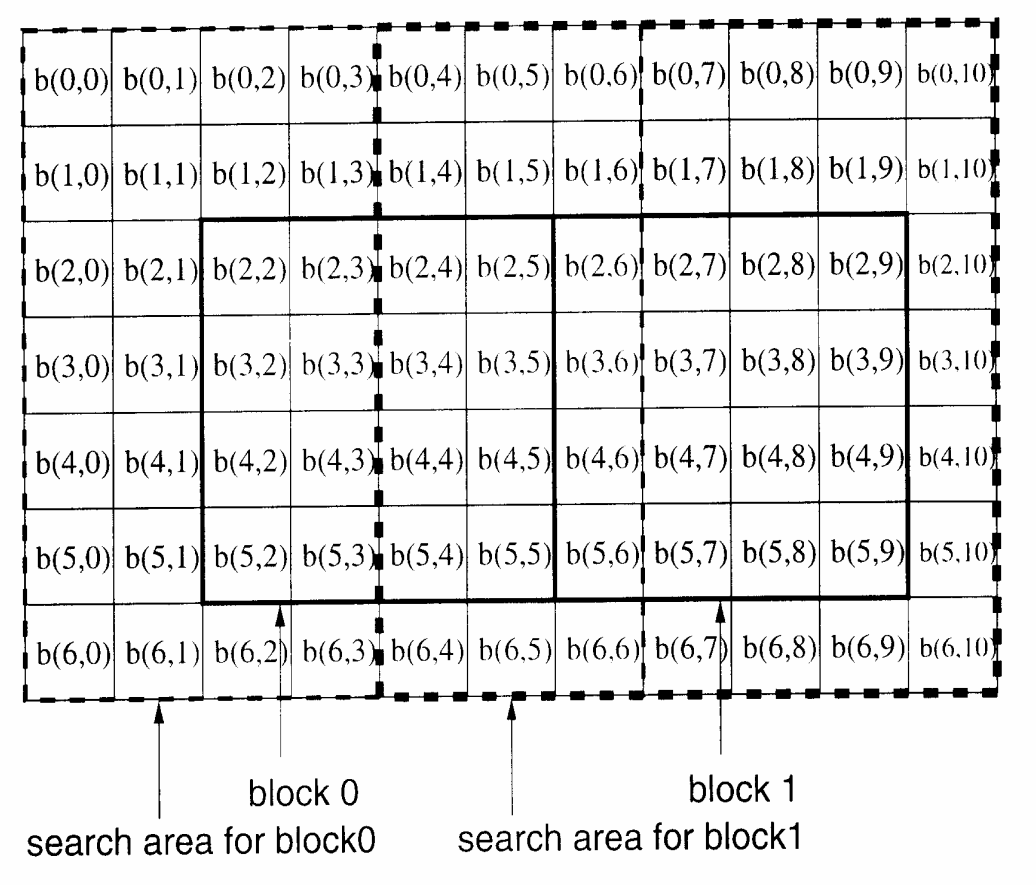
- 4x4 current block

a(0,0)	a(0,1)	a(0,2)	a(0,3)
a(1,0)	a(1,1)	a(1,2)	a(1,3)
a(2,0)	a(2,1)	a(2,2)	a(2,3)
a(3,0)	a(3,1)	a(3,2)	a(3,3)

column-scan order

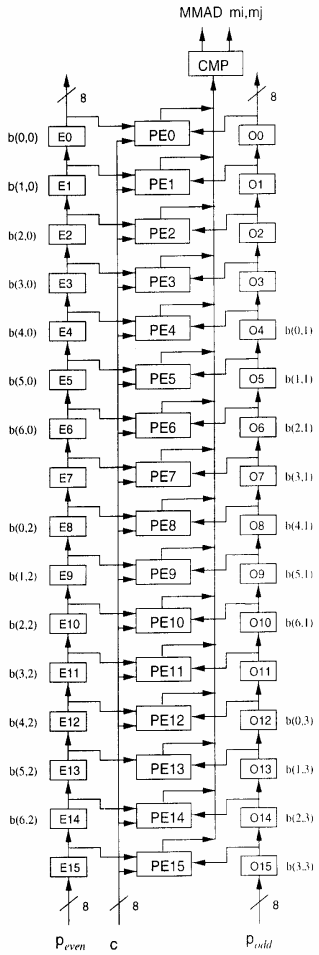


7x7 Search Area

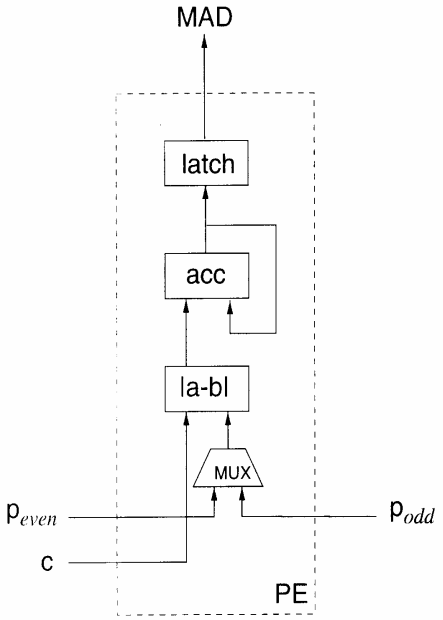


Data-Interlacing Architecture

- $(N = 4, p =$



(a)



(b)

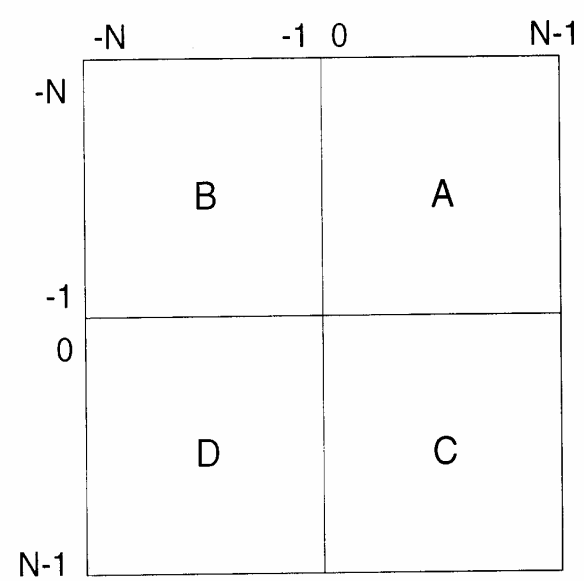
Data Flow for FSBMA

- $(N = 4, p = 2)$

Cycle Time	Data Sequence	PE0	PE1	.	PE14	PE15
0× 16+0	a(0,0)	a(0,0)-b(0,0)	a(0,0)-b(1,0)	.	a(0,0)-b(2,3)	a(0,0)-b(3,3)
0× 16+1	a(1,0)	a(1,0)-b(1,0)	a(1,0)-b(2,0)	.	a(1,0)-b(3,3)	a(1,0)-b(4,3)
...	...	...	...	.	...	...
...	...	...	...	.	...	...
0×16+14	a(2,3)	a(2,3)-b(2,3)	a(2,3)-b(3,3)	.	a(2,3)-b(4,6)	a(2,3)-b(5,6)
0×16+15	a(3,3)	a(3,3)-b(3,3)	a(3,3)-b(4,3)	.	a(3,3)-b(5,6)	a(3,3)-b(6,6)
1× 16+0	a(0,0)	a(0,0)-b(0,4)	a(0,0)-b(1,4)	.	a(0,0)-b(2,7)	a(0,0)-b(3,7)
1× 16+1	a(1,0)	a(1,0)-b(1,4)	a(1,0)-b(2,4)	.	a(1,0)-b(3,7)	a(1,0)-b(4,7)
...	...	...	...	.	...	...
...	...	...	...	.	...	...
1×16+14	a(2,3)	a(2,3)-b(2,7)	a(2,3)-b(3,7)	.	a(2,3)-b(4,10)	a(2,3)-b(5,10)
1×16+15	a(3,3)	a(3,3)-b(3,7)	a(3,3)-b(4,7)	.	a(3,3)-b(5,10)	a(3,3)-b(6,10)
...	...	...	...	.	...	...
...	...	...	...	.	...	...
NEXT						
...	...	...	...	.	...	...
...	...	...	...	.	...	...

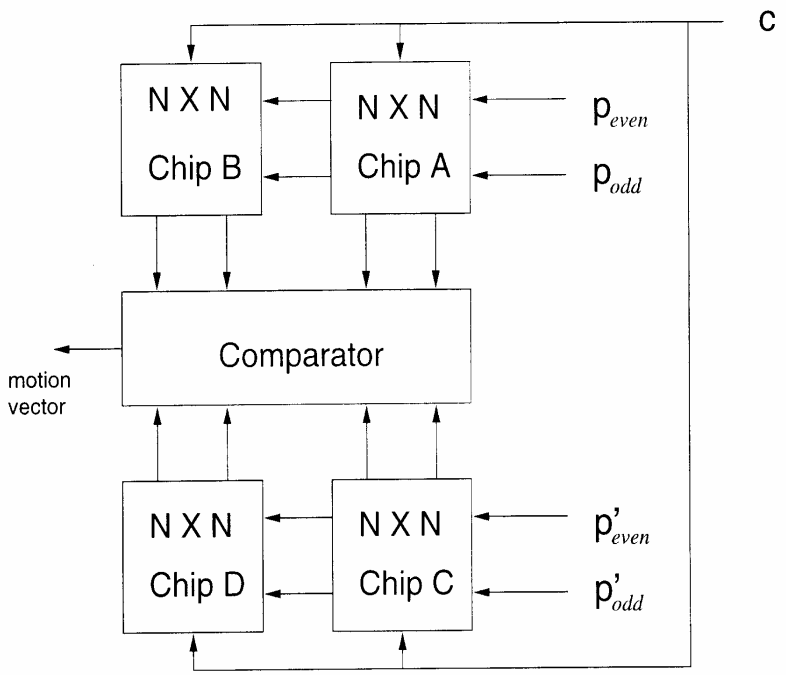
Current Block : NxN
Search Area : -N to N-1

- (a)4 sub-search area



(a)

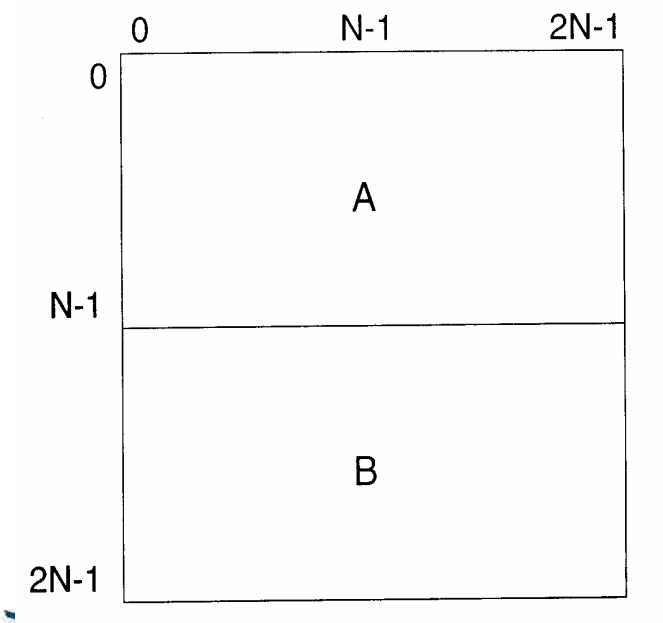
(b)Block Diagram for cascading 4 chips



(b)

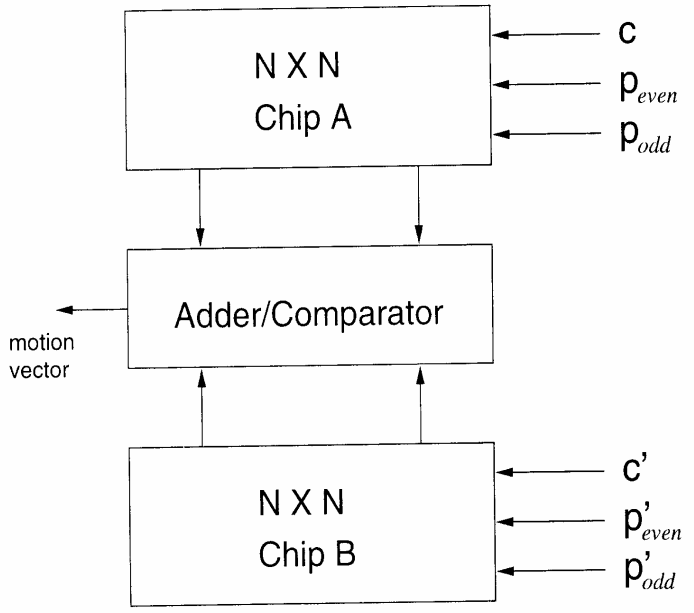
Current Block : 2Nx2N
Search Area : -N/2 to N/2-1

- (a)2 sub-blocks



(a)

(b)Block Diagram for cascading 2 chips



(b)

Comparison with other architectures

- $(N = 16, p = 8)$

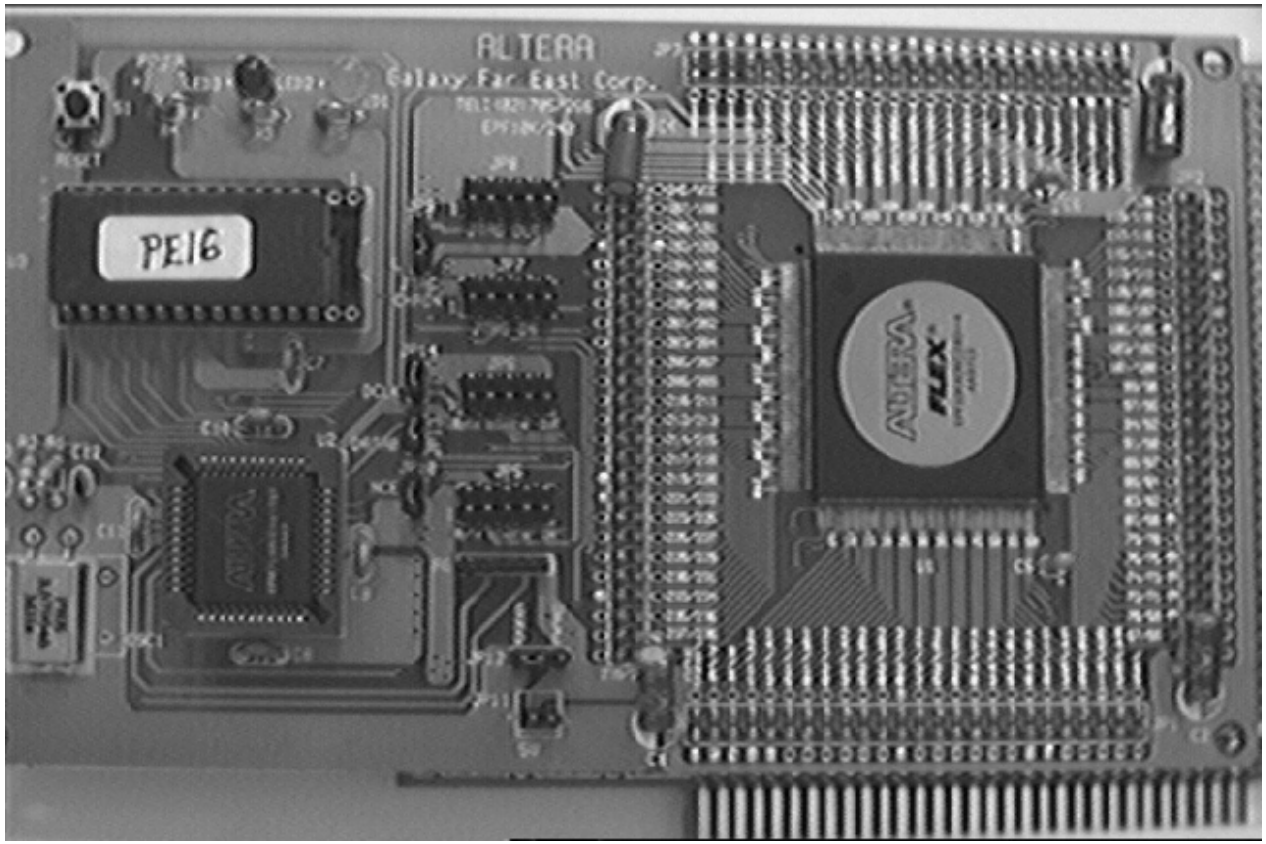
Architecture	[1]	[2]	[3]	[4]	[5]	[6]	proposed architecture
No. of input data pins	24	24	24	16	136	24	24
No. of PEs	16	16	256	256	256	256	256
Clock cycles/block	4096	4096	256	961	496	256	256
Throughput(blocks/cycles)	$\frac{1}{4096}$	$\frac{1}{4096}$	$\frac{1}{256}$	$\frac{1}{961}$	$\frac{1}{496}$	$\frac{1}{256}$	$\frac{1}{256}$
PE utilization	100%	100%	100%	26.6%	100%	100%	100%
No. of data accesses	12288	12032	752	1217	8192	768	752
Cascadable ?	Yes	Yes	No	No	No	Yes	Yes

Comparison with other architectures

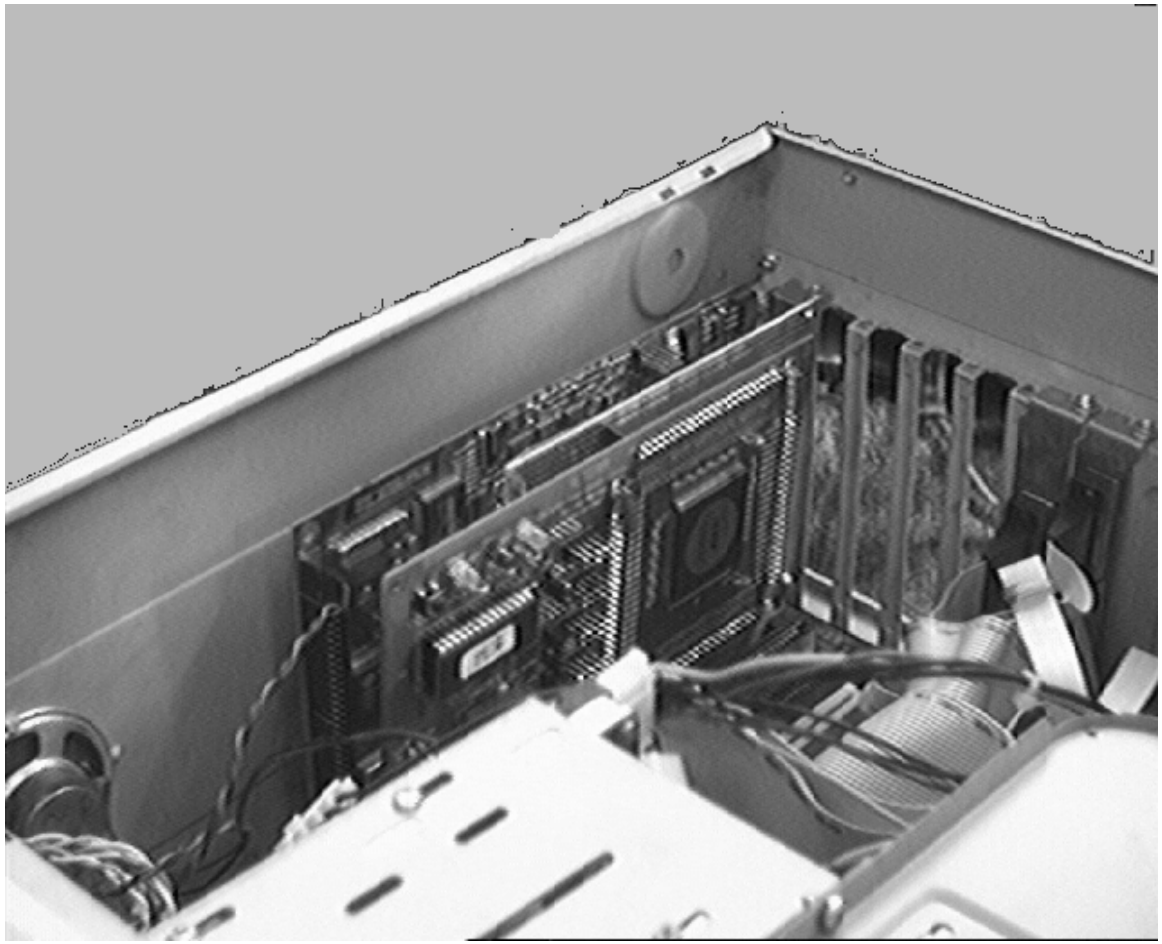
- $(N = 16, p = 16)$

Architecture	[1]	[2]	[3]	[4]	[5]	[6]	proposed architecture
No. of input data pins	48	32	24	16	136	72	40
No. of PEs	64	64	256	256	256	1024	1024
Clock cycles/block	4096	4096	1024	2209	1504	256	256
Throughput(blocks/cycles)	$\frac{1}{4096}$	$\frac{1}{4096}$	$\frac{1}{1024}$	$\frac{1}{2209}$	$\frac{1}{1504}$	$\frac{1}{256}$	$\frac{1}{256}$
PE utilization	100%	100%	100%	46.6%	100%	100%	100%
No. of data accesses	32768	32256	1008	2465	24320	2304	1248

Board for Motion Estimation

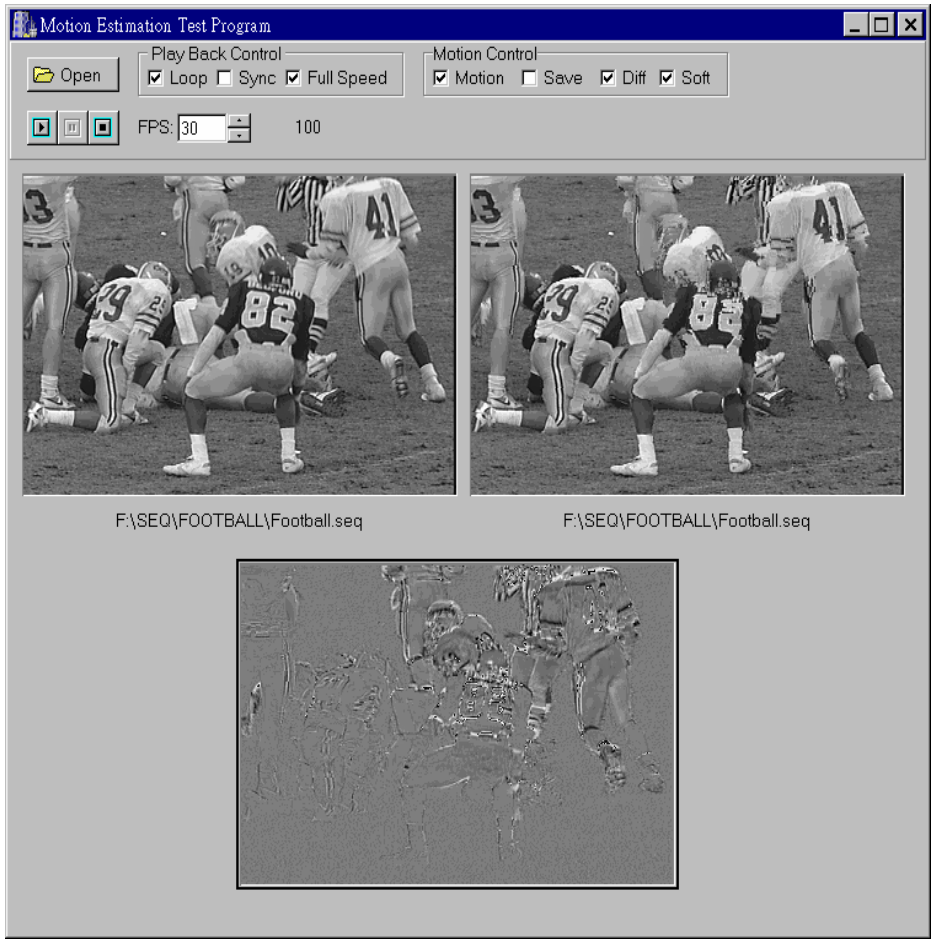


Board for Motion Estimation

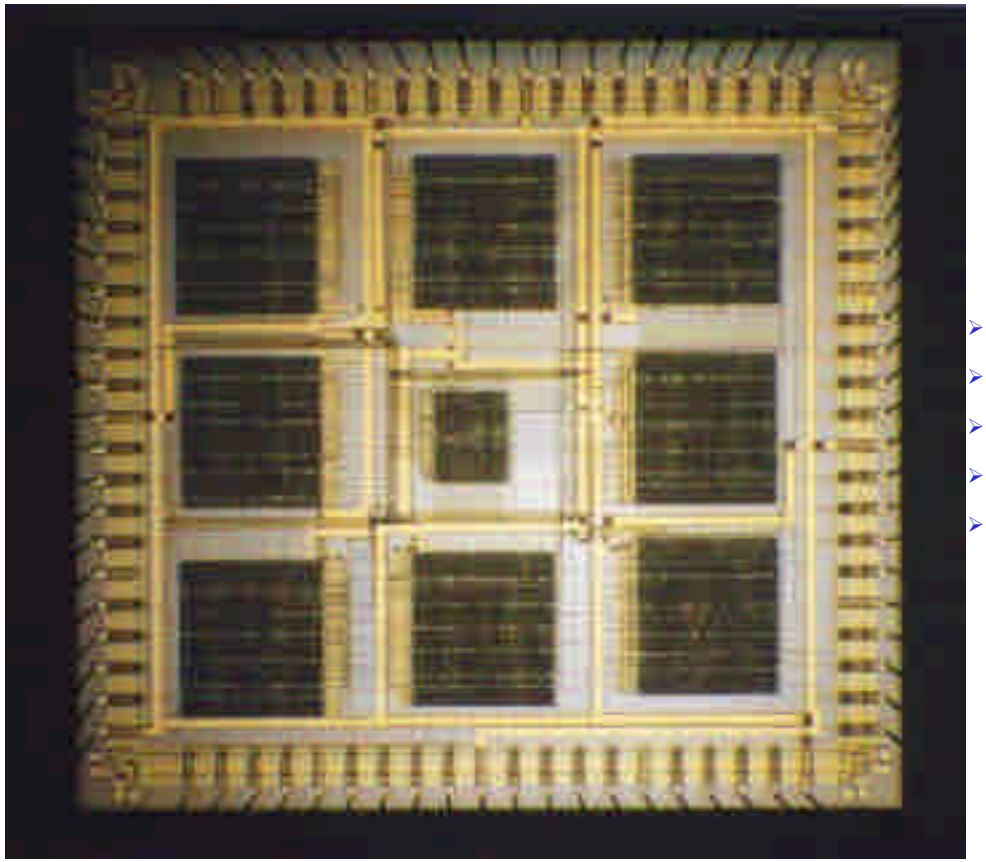


Demonstration for Table Tennis

Demonstration for Football

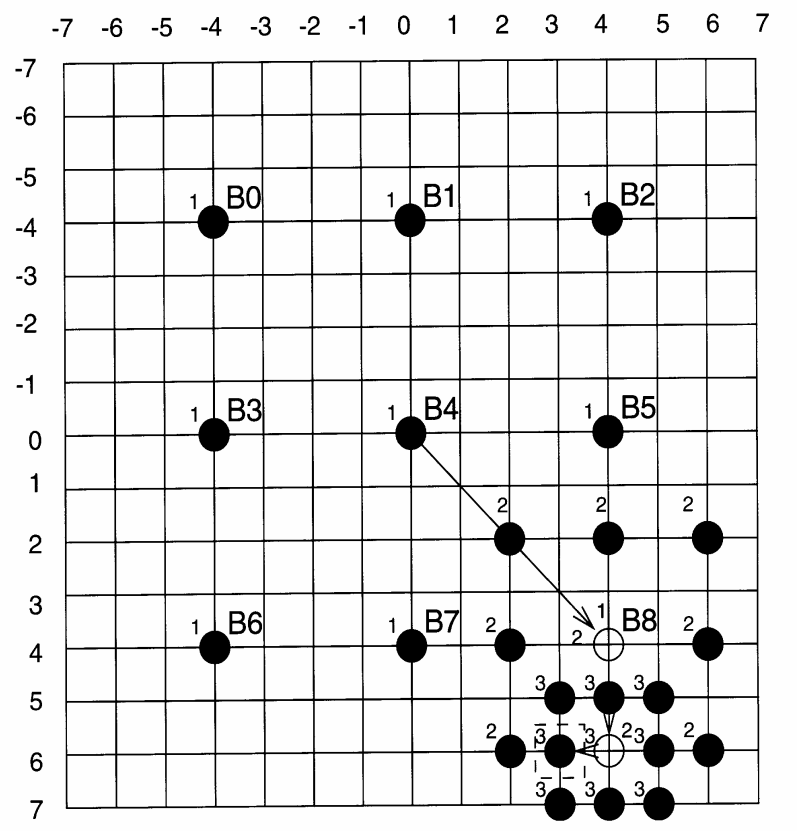


Chip Layout

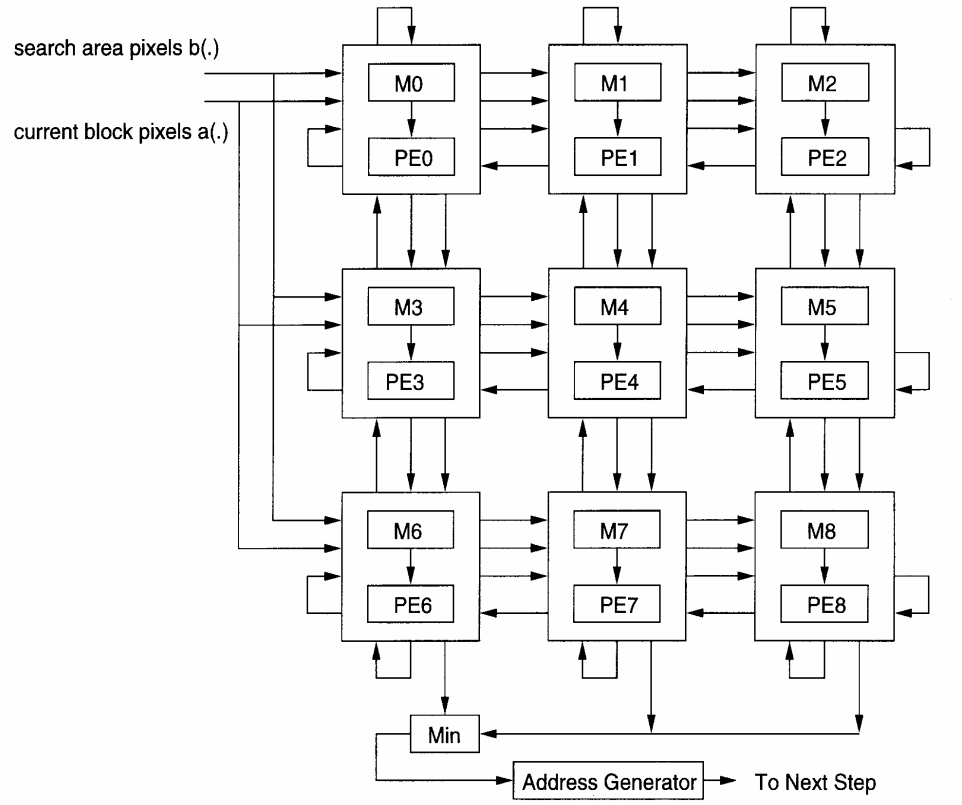


- Technology: COMPASS 0.6 μm CMOS
- Die Size: 7.5 mm x 6.7 mm
- Number of Transistors: 220604
- Number of Pins: 81
- Clock Rate: 12.5 MHz

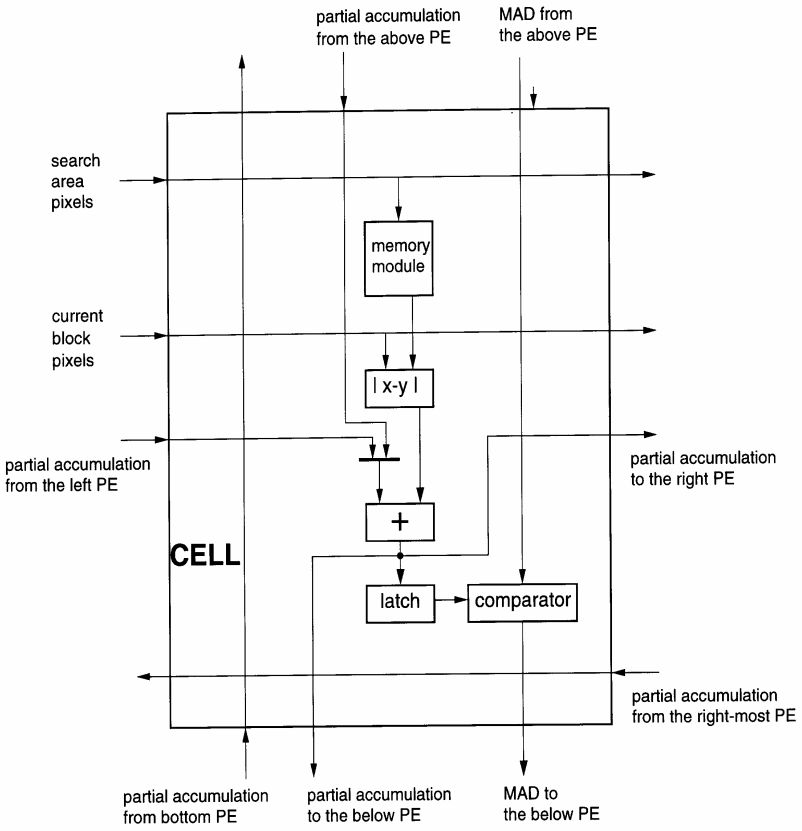
3-Step Hierarchical Search BMA



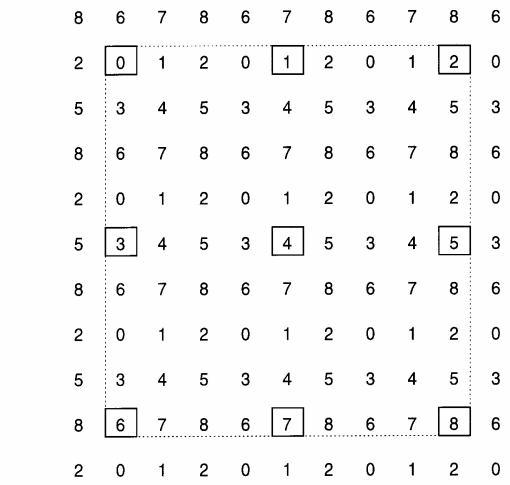
9-cells Architecture with Data-Rings



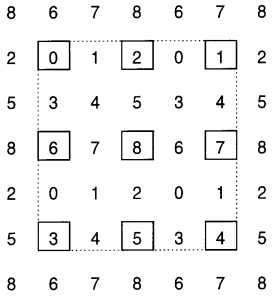
Architecture of the Cell



Distribution of the Search Area



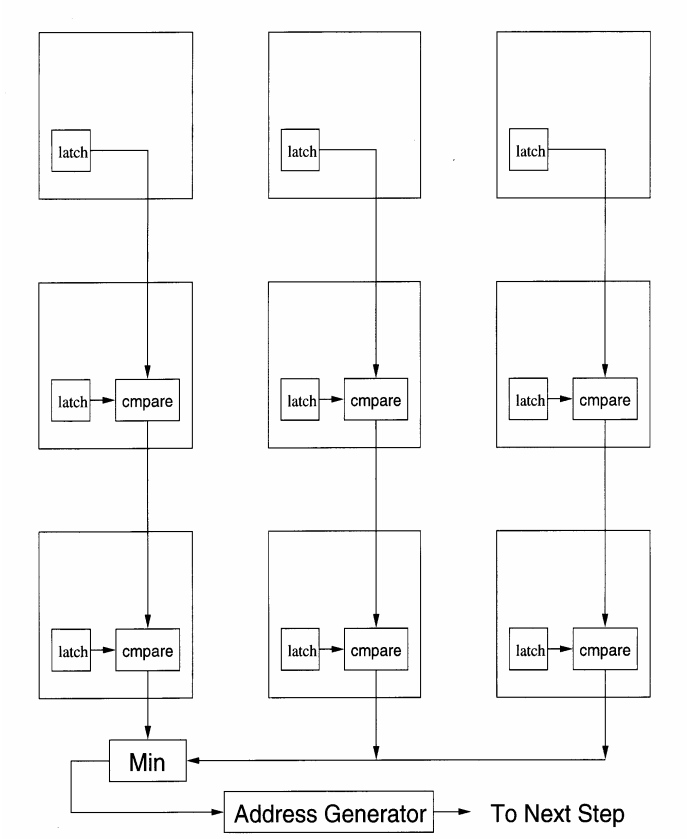
(a)



(b)

(c)

Miminmum MAD Extraction



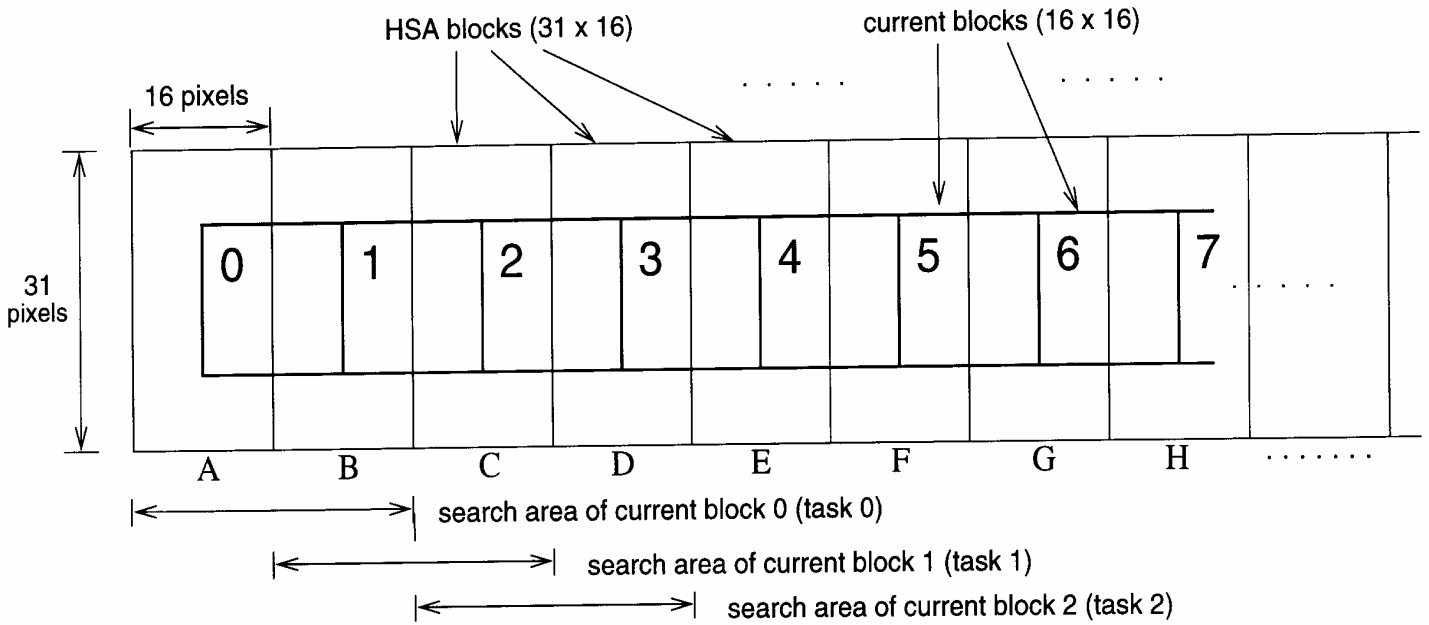
Data Flow for Step1 and Step3

Cycle time	Data Sequence	$PE0$	$PE1$	$PE2$	$PE3$	$PE4$	$PE5$	$PE6$	$PE7$	$PE8$
0×16+0	a(0,0)	B0	B1	B2	B3	B4	B5	B6	B7	B8
0×16+1	a(0,1)	B2	B0	B1	B5	B3	B4	B8	B6	B7
0×16+2	a(0,2)	B1	B2	B0	B4	B5	B3	B7	B8	B6
0×16+3	a(0,3)	B0	B1	B2	B3	B4	B5	B6	B7	B8
0×16+4	a(0,4)	B2	B0	B1	B5	B3	B4	B8	B6	B7
0×16+5	a(0,5)	B1	B2	B0	B4	B5	B3	B7	B8	B6
0×16+6	a(0,6)	B0	B1	B2	B3	B4	B5	B6	B7	B8
0×16+7	a(0,7)	B2	B0	B1	B5	B3	B4	B8	B6	B7
0×16+8	a(0,8)	B1	B2	B0	B4	B5	B3	B7	B8	B6
0×16+9	a(0,9)	B0	B1	B2	B3	B4	B5	B6	B8	B8
0×16+10	a(0,10)	B2	B0	B1	B5	B3	B4	B8	B6	B7
0×16+11	a(0,11)	B1	B2	B0	B4	B5	B3	B7	B8	B6
0×16+12	a(0,12)	B0	B1	B2	B3	B4	B5	B6	B7	B8
0×16+13	a(0,13)	B2	B0	B1	B5	B3	B4	B8	B6	B7
0×16+14	a(0,14)	B1	B2	B0	B4	B5	B3	B7	B8	B6
0×16+15	a(0,15)	B0	B1	B2	B3	B4	B5	B6	B7	B8
1×16+0	a(1,0)	B6	B7	B8	B0	B1	B2	B3	B4	B5
1×16+1	a(1,1)	B8	B6	B7	B2	B0	B1	B5	B3	B4
...	...	...	...			...			...	...
...	...	...	...			...			...	...
1×16+14	a(1,14)	B7	B8			...			B5	B3
1×16+15	a(1,15)	B6	B7			...			B4	B5
...	...	...	...			...			...	...
...	...	...	...			...			...	...
...	...	...	...			...			...	...
...	...	...	...			...			...	...
14×16+0	a(14,0)	B3	B4			...			B1	B2
14×16+1	a(14,1)	B5	B3			...			B0	B1
...	...	...	...			...			...	...
14×16+14	a(14,14)	B4	B5			...			B2	B0
14×16+15	a(14,15)	B3	B4			...			B1	B2
15×16+0	a(15,0)	B0	B1			...			B7	B8
15×16+1	a(15,1)	B2	B0			...			B6	B7
...	...	...	...			...			...	...
...	...	...	...			...			...	...
15×16+14	a(15,14)	B1	B2			...			B8	B6
15×16+15	a(15,15)	B0	B1			...			B7	B8

Data Flow for Step2

Cycle time	Data Sequence	$PE0$	$PE1$	$PE2$	$PE3$	$PE4$	$PE5$	$PE6$	$PE7$	$PE8$
0×16+0	a(0,0)	B0	B2	B1	B6	B4	B7	B3	B5	B4
0×16+1	a(0,1)	B1	B0	B2	B7	B6	B4	B4	B3	B5
0×16+2	a(0,2)	B2	B1	B0	B4	B7	B6	B5	B4	B3
0×16+3	a(0,3)	B0	B2	B1	B6	B4	B7	B3	B5	B4
0×16+4	a(0,4)	B1	B0	B2	B7	B6	B4	B4	B3	B5
0×16+5	a(0,5)	B2	B1	B0	B4	B7	B6	B5	B4	B3
0×16+6	a(0,6)	B0	B2	B1	B6	B4	B7	B3	B5	B4
0×16+7	a(0,7)	B1	B0	B2	B7	B6	B4	B4	B3	B5
0×16+8	a(0,8)	B2	B1	B0	B4	B7	B6	B5	B4	B3
0×16+9	a(0,9)	B0	B2	B1	B6	B4	B7	B3	B4	B4
0×16+10	a(0,10)	B1	B0	B2	B7	B6	B4	B4	B3	B5
0×16+11	a(0,11)	B2	B1	B0	B4	B7	B6	B5	B4	B3
0×16+12	a(0,12)	B0	B2	B1	B6	B4	B7	B3	B5	B4
0×16+13	a(0,13)	B1	B0	B2	B7	B6	B4	B4	B3	B5
0×16+14	a(0,14)	B2	B1	B0	B4	B7	B6	B5	B4	B3
0×16+15	a(0,15)	B0	B2	B1	B6	B4	B7	B3	B5	B4
1×16+0	a(1,0)	B3	B5	B4	B0	B2	B1	B6	B4	B7
1×16+1	a(1,1)	B4	B3	B5	B1	B0	B2	B7	B6	B4
...	...	...	...			...			...	...
...	...	...	...			...			...	...
1×16+14	a(1,14)	B5	B4			...			B7	B6
1×16+15	a(1,15)	B3	B5			...			B4	B7
...	...	...	...			...			...	...
...	...	...	...			...			...	...
...	...	...	...			...			...	...
...	...	...	...			...			...	...
14×16+0	a(14,0)	B6	B4			...			B2	B1
14×16+1	a(14,1)	B7	B6			...			B0	B2
...	...	...	...			...			...	...
14×16+14	a(14,14)	B4	B7			...			B1	B0
14×16+15	a(14,15)	B6	B4			...			B2	B1
15×16+0	a(15,0)	B0	B2			...			B5	B4
15×16+1	a(15,1)	B1	B0			...			B3	B5
...	...	...	...			...			...	...
...	...	...	...			...			...	...
15×16+14	a(15,14)	B2	B1			...			B4	B3
15×16+15	a(15,15)	B0	B2			...			B5	B4

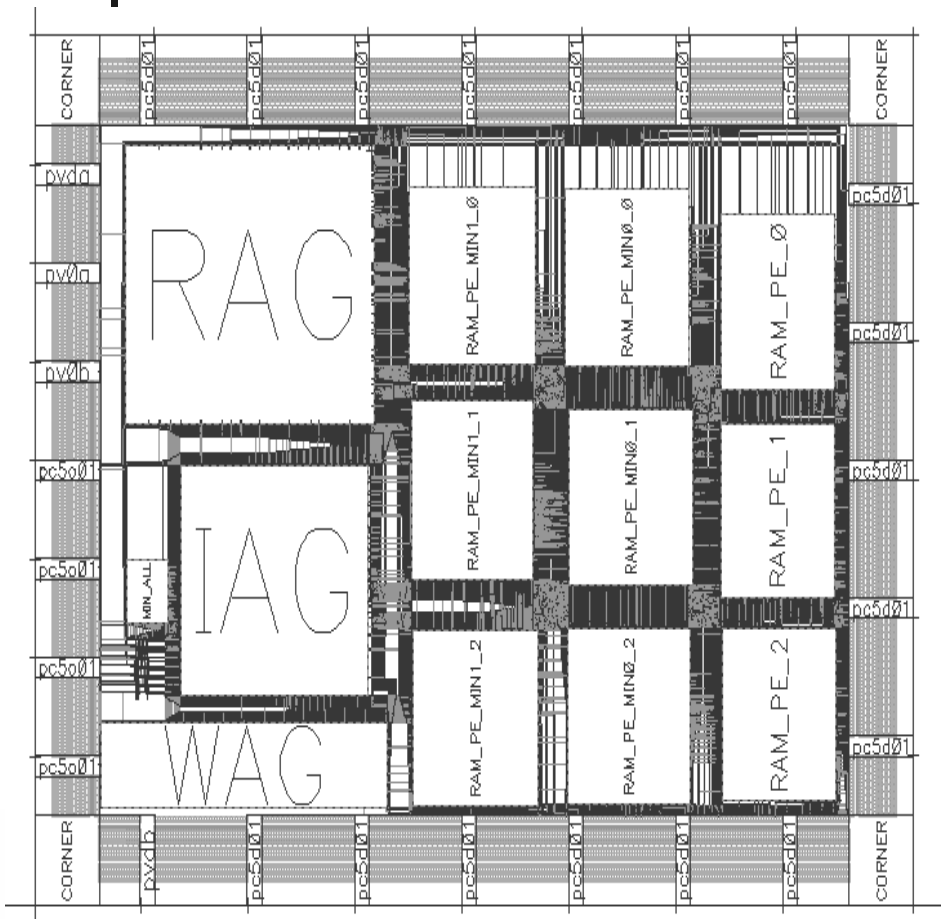
Overlap for the Search Area Adjacent Current Blocks



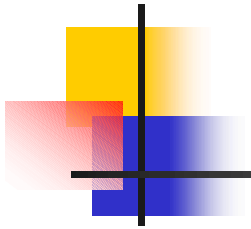
Comparison with other architectures

Architecture	proposed architecture	architecture in [5]	architecture in [6]		
			Type I	Type II	Type III
Input data ports	16	136	40	132	416
No. of the used PE's	9	9	9	36	144
Clock cycles per block matching	783	1280	798	237	129
Throughput	$\frac{1}{783}$	$\frac{1}{1280}$	$\frac{1}{798}$	$\frac{1}{237}$	$\frac{1}{129}$
$\frac{Throughput}{No.\ of\ the\ used\ PE's}$	$\frac{1}{7047}$	$\frac{1}{11520}$	$\frac{1}{7182}$	$\frac{1}{8532}$	$\frac{1}{18576}$

Chip Layout



- **Technology: COMPASS 0.6 μm CMOS**
- **Die Size: 6.67 mm x 4.69 mm**
- **Number of Transistors: 25636**
- **Number of Pins: 26**
- **Clock Rate: 50 MHz**



Conclusion

- Software Solution
- Hardware Solution (VLSI)